National Semiconductor

GAL20V8/A 24-Pin Generic Array Logic Family

General Description

The EECMOS GAL® 20V8/A devices are fabricated using electrically erasable floating gate technology. This programmable memory technology applied to array logic provides designers with reconfigurable logic and bipolar performance at significantly reduced power levels.

The 24-pin GAL20V8 features 8 programmable Output Logic Macrocells (OLMCs) allowing each TRI-STATE® output to be configured by the user. Additionally, the GAL20V8 is capable of emulating, in a functional/fuse map/parametric compatible device, the most popular 24-pin PAL® device architectures.

Programming is accomplished using readily available hardware and software tools. NSC guarantees a minimum 100 erase/write cycles.

Unique test circuitry and reprogrammable cells allow complete AC, DC, cell and functionality testing during manufacture. Therefore, NSC guarantees 100% field programmability of the GAL devices. In addition, electronic signature is available to provide positive device ID. A security circuit is built-in, providing proprietary designs with copy protection.

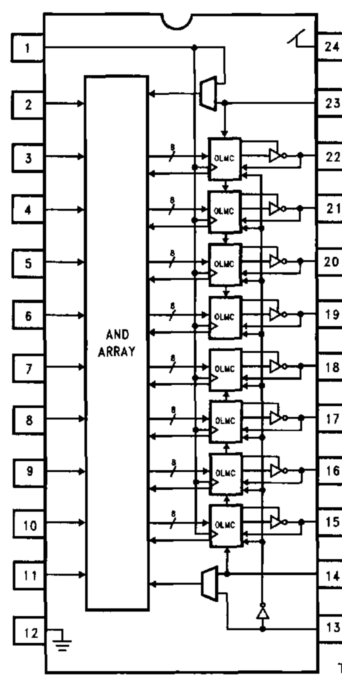
Features

- High performance EECMOS technology
  - 7.5 ns maximum propagation delay
  - f_{CLK} = 100 MHz
  - 5 ns maximum from clock input to data output
  - TTL compatible 24 mA outputs
- Reduced power
  - Low power = 115 mA I_{CC} max, 75 mA typ
- Electrically erasable cell technology
  - Reconfigurable logic
  - Reprogrammable cells
  - 100% tested/guaranteed 100% yields
  - High speed electrical erasure (<50 ms)
  - 20 year data retention
- Eight output logic macrocells
  - Maximum flexibility for complex logic designs
  - Programmable output polarity
  - Also emulates 24-pin PAL devices with full function/fuse map/parametric compatibility
- Preload and power-up reset of all registers
  - 100% functional testability
- Fully supported by National OPAL™ and OPALjr development software
- Security cell prevents copying logic

PAL Replacement by Device Type

"Small PAL" Mode				"Registered PAL" Mode			"Medium PAL" Mode
14L8	16L6	18L4	20L2	20R8	20R6	20R4	20L8
14H8	16H6	18H4	20H2	20RP8	20RP6	20RP4	20H8
14P8	16P6	18P4	20P2				20P8

Block Diagram—GAL20V8



TL/L/11256-1

GAL20V8-7/-10

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
Input Voltage (Note 2)	−2.5V to V_{CC} + 1.0V
Off-State Output Voltage (Note 2)	−2.5V to V_{CC} + 1.0V
Output Current	±100 mA
Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−65°C to +125°C
Junction Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C
ESD Tolerance	>2000V

C_{ZAP} = 100 pF
R_{ZAP} = 1500Ω
Test Method: Human Body Model
Test Specification: NSC SOP-5-028 Rev. C

Recommended Operating Conditions

SUPPLY VOLTAGE AND TEMPERATURE

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
T_A	Operating Free-Air Temperature	0	25	75	°C
T_C	Operating Case Temperature				°C

AC TIMING REQUIREMENTS

Symbol	Parameter		GAL20V8-7L		GAL20V8-10L		Units
			Min	Max	Min	Max	
t_{SU}	Set-Up Time (Input or Feedback before Clock)		7		10		ns
t_H	Hold Time (Input after Clock)		0		0		ns
t_w	Clock Pulse Width (High/Low)		5		8		ns
t_{CYCLE}	Clock Cycle Period (with Feedback) (Note 3)		12		17		ns
f_{CLK}	Clock Frequency (Note 4)	With Feedback		83.3		58.8	MHz
		Without Feedback		100		62.5	MHz
f_I	Input Frequency (Note 5)			133.3		100	MHz
t_{PR}	Clock Valid after Power-Up			100		100	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

Note 2: Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

Note 3: $t_{CYCLE} = t_{SU} + t_{CLK}$

Note 4: f_{CLK} (with feedback) = $(t_{CYCLE})^{-1}$
f_{CLK} (without feedback) = $(2\ t_w)^{-1}$

Note 5: $f_I = (t_{PD})^{-1}$

GAL20V8-7/-10

Electrical Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2.0		$V_{CC} + 1$	V
V_{IL}	Low Level Input Voltage			−0.5		0.8	V
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −3.2 mA	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 24 mA			0.5	V
I_{OZH}	High Level Off State Output Current	V_{CC} = Max, V_O = V_{CC} (Max)				10	μA
I_{OZL}	Low Level Off State Output Current	V_{CC} = Max, V_O = GND				−10	μA
I_I	Maximum Input Current	V_{CC} = Max, V_I = V_{CC} (Max)				10	μA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = V_{CC} (Max)				10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = GND				−10	μA
I_{OS}*	Output Short Circuit Current	V_{CC} = 5.0V, V_O = GND		−30		−150	mA
I_{CC}	Supply Current	f = 25 MHz, V_{CC} = Max			75	115	mA
C_I	Input Capacitance	V_{CC} = 5.0V, V_I = 2.0V			5	8	pF
$C_{I/O}$	I/O Capacitance	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V			5	8	pF

*One output at a time for a maximum duration of one second.

Switching Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Conditions	GAL20V8-7		GAL20V8-10		Units
			Min	Max	Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output	S1 Closed, C_L = 50 pF		7.5		10	ns
t_{CLK}	Clock to Registered Output or Feedback	S1 Closed, C_L = 50 pF		5		7	ns
t_{PZXG}	$\overline{G}$ ↓ to Registered Output Enabled	Active High; S1 Open, C_L = 50 pF Active Low; S1 Closed, C_L = 50 pF		6		10	ns
t_{PXZG}	$\overline{G}$ ↑ to Registered Output Disabled	From V_{OH}; S1 Open, C_L = 5 pF From V_{OL}; S1 Closed, C_L = 5 pF		6		10	ns
t_{PZXI}	Input to Combinatorial Output Enabled via Product Term	Active High; S1 Open, C_L = 50 pF Active Low; S1 Closed, C_L = 50 pF		9		10	ns
t_{PXZI}	Input to Combinatorial Output Disabled via Product Term	From V_{OH}; S1 Open, C_L = 5 pF From V_{OL}; S1 Closed, C_L = 5 pF		9		10	ns
t_{RESET}	Power-Up to Registered Output High	S1 Closed, C_L = 50 pF		45		45	μs

GAL20V8A-12/-15

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
Input Voltage (Note 2)	−2.5V to V_{CC} + 1.0V
Off-State Output Voltage (Note 2)	−2.5V to V_{CC} + 1.0V
Output Current	±100 mA
Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−65°C to +125°C
Junction Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C
ESD Tolerance	1000V

C_{ZAP} = 100 pF
R_{ZAP} = 1500Ω
Test Method: Human Body Model
Test Specification: NSC SOP-5-028 Rev. C

Recommended Operating Conditions

SUPPLY VOLTAGE AND TEMPERATURE

Symbol	Parameter	Commercial			Industrial			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	4.5	5	5.5	V
T_A	Operating Free-Air Temperature	0	25	75	−40	25	85	°C

AC TIMING REQUIREMENTS

Symbol	Parameter		GAL20V8A-12L		GAL20V8A-15L		Units
			COM		COM/IND		
			Min	Max	Min	Max	
t_{SU}	Set-Up Time (Input or Feedback before Clock)		10		12		ns
t_H	Hold Time (Input after Clock)		0		0		ns
t_w	Clock Pulse Width (High/Low)		8		8		ns
t_{CYCLE}	Clock Cycle Period (with Feedback) (Note 3)		20		22		ns
f_{CLK}	Clock Frequency (Note 4)	With Feedback		50		45.5	MHz
		Without Feedback		62.5		62.5	MHz
f_I	Input Frequency (Note 5)			83.3		66.6	MHz
t_{PR}	Clock Valid after Power-Up			100		100	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

Note 2: Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

Note 3: $t_{CYCLE} = t_{SU} + t_{CLK}$

Note 4: f_{CLK} (with feedback) = $(t_{CYCLE})^{-1}$
f_{CLK} (without feedback) = $(2\ t_w)^{-1}$

Note 5: $f_I = (t_{PD})^{-1}$

GAL20V8A-12/-15

Electrical Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Conditions		Temperature Range	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage				2.0		$V_{CC} + 1$	V
V_{IL}	Low Level Input Voltage				−0.5		0.8	V
V_{OH}	High Level Output Voltage	V_{CC} = Min	$I_{OH} = -3.2$ mA		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 24 mA				0.5	V
I_{OZH}	High Level Off State Output Current	V_{CC} = Max, $V_O = V_{CC}$ (Max)					10	μA
I_{OZL}	Low Level Off State Output Current	V_{CC} = Max, V_O = GND					−10	μA
I_I	Maximum Input Current	V_{CC} = Max, $V_I = V_{CC}$ (Max)					10	μA
I_{IH}	High Level Input Current	V_{CC} = Max, $V_I = V_{CC}$ (Max)					10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = GND					−10	μA
I_{OS}*	Output Short Circuit Current	V_{CC} = 5.0V, V_O = GND			−30		−150	mA
I_{CC}	Supply Current	f = 25 MHz, V_{CC} = Max		COM			90	mA
				IND			130	mA
C_I	Input Capacitance	V_{CC} = 5.0V, V_I = 2.0V					8	pF
$C_{I/O}$	I/O Capacitance	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V					10	pF

*One output at a time for a maximum duration of one second.

Switching Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Conditions	GAL20V8A-12L		GAL20V8A-15L		Units
			COM		COM/IND		
			Min	Max	Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output	S1 Closed, C_L = 50 pF		12		15	ns
t_{CLK}	Clock to Registered Output or Feedback	S1 Closed, C_L = 50 pF		10		10	ns
t_{PZXG}	$\overline{G}$ ↓ to Registered Output Enabled	Active High; S1 Open, C_L = 50 pF Active Low; S1 Closed, C_L = 50 pF		10		15	ns
t_{PXZG}	$\overline{G}$ ↑ to Registered Output Disabled	From V_{OH}; S1 Open, C_L = 5 pF From V_{OL}; S1 Closed, C_L = 5 pF		10		15	ns
t_{PZXI}	Input to Combinatorial Output Enabled via Product Term	Active High; S1 Open, C_L = 50 pF Active Low; S1 Closed, C_L = 50 pF		12		15	ns
t_{PXZI}	Input to Combinatorial Output Disabled via Product Term	From V_{OH}; S1 Open, C_L = 5 pF From V_{OL}; S1 Closed, C_L = 5 pF		12		15	ns
t_{RESET}	Power-Up to Registered Output High	S1 Closed, C_L = 50 pF		45		45	μs

GAL20V8-20/-25

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
Input Voltage (Note 2)	−2.5V to V_{CC} + 1.0V
Off-State Output Voltage (Note 2)	−2.5V to V_{CC} + 1.0V
Output Current	±100 mA
Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−65°C to +125°C
Junction Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C
ESD Tolerance	1000V

C_{ZAP} = 100 pF
R_{ZAP} = 1500Ω
Test Method: Human Body Model
Test Specification: NSC SOP-5-028 Rev. C

Recommended Operating Conditions

SUPPLY VOLTAGE AND TEMPERATURE

Symbol	Parameter	Commercial			Industrial			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	4.5	5	5.5	V
T_A	Operating Free-Air Temperature	0	25	75	−40	25	85	°C

AC TIMING REQUIREMENTS

Symbol	Parameter		GAL20V8-20L		GAL20V8-25L		GAL20V8-25Q		Units
			COM		COM		COM		
			Min	Max	Min	Max	Min	Min	
t_{SU}	Set-Up Time (Input or Feedback before Clock)		15		15		15		ns
t_H	Hold Time (Input after Clock)		0		0		0		ns
t_W	Clock Pulse Width (High/Low)		12		12		12		ns
t_{CYCLE}	Clock Cycle Period (with Feedback) (Note 3)		27		27		27		ns
f_{CLK}	Clock Frequency (Note 4)	With Feedback		37		37		37	MHz
		Without Feedback		41.66		41.66		41.66	MHz
f_I	Input Frequency (Note 5)			50		50		50	MHz
t_{PR}	Clock Valid after Power-Up			100		100		100	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

Note 2: Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

Note 3: $t_{CYCLE} = t_{SU} + t_{CLK}$

Note 4: f_{CLK} (with feedback) = $(t_{CYCLE})^{-1}$
f_{CLK} (without feedback) = $(2\ t_W)^{-1}$

Note 5: $f_I = (t_{PD})^{-1}$

GAL20V8-20/-25

Electrical Characteristics Over Recommended Operating Conditions

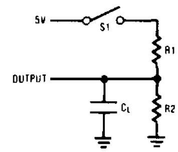
Symbol	Parameter	Conditions		Temperature Range	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage				2.0		$V_{CC} + 1$	V
V_{IL}	Low Level Input Voltage				−0.5		0.8	V
V_{OH}	High Level Output Voltage	V_{CC} = Min	$I_{OH} = -3.2$ mA		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min	$I_{OL} = 24$ mA				0.5	V
I_{OZH}	High Level Off State Output Current	V_{CC} = Max, $V_O = V_{CC}$ (Max)					10	μA
I_{OZL}	Low Level Off State Output Current	V_{CC} = Max, V_O = GND					−10	μA
I_I	Maximum Input Current	V_{CC} = Max, $V_I = V_{CC}$ (Max)					10	μA
I_{IH}	High Level Input Current	V_{CC} = Max, $V_I = V_{CC}$ (Max)					10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = GND					−10	μA
I_{OS}*	Output Short Circuit Current	V_{CC} = 5.0V, V_O = GND			−30		−150	mA
I_{CC}	Supply Current	f = 25 MHz, V_{CC} = Max	-20L, -25L				90	mA
			-25Q				55	mA
C_I	Input Capacitance	V_{CC} = 5.0V, V_I = 2.0V					8	pF
$C_{I/O}$	I/O Capacitance	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V					10	pF

*One output at a time for a maximum duration of one second.

Switching Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Conditions	GAL20V8-20L		GAL20V8-25L		GAL20V8-25Q		Units
			COM		COM		COM		
			Min	Max	Min	Max	Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output	S1 Closed, C_L = 50 pF		20		25		25	ns
t_{CLK}	Clock to Registered Output or Feedback	S1 Closed, C_L = 50 pF		12		12		12	ns
t_{PZXG}	$\overline{G}$ ↓ to Registered Output Enabled	Active High; S1 Open, C_L = 50 pF Active Low; S1 Closed, C_L = 50 pF		18		20		20	ns
t_{PXZG}	$\overline{G}$ ↑ to Registered Output Disabled	From V_{OH}; S1 Open, C_L = 5 pF From V_{OL}; S1 Closed, C_L = 5 pF		18		20		20	ns
t_{PZXI}	Input to Combinatorial Output Enabled via Product Term	Active High; S1 Open, C_L = 50 pF Active Low; S1 Closed, C_L = 50 pF		20		25		25	ns
t_{PXZI}	Input to Combinatorial Output Disabled via Product Term	From V_{OH}; S1 Open, C_L = 5 pF From V_{OL}; S1 Closed, C_L = 5 pF		20		25		25	ns
t_{RESET}	Power-Up to Registered Output High	S1 Closed, C_L = 50 pF		45		45		45	μs

AC Test Load



COM'L/IND
R1 = 200
R2 = 390

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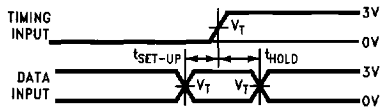
Test Waveforms

Setup and Hold



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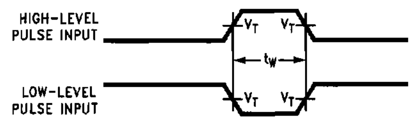
Pulse Width



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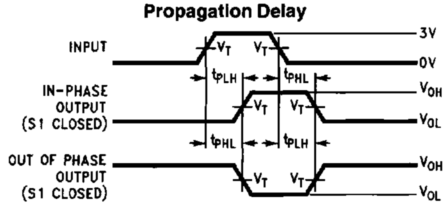
Propagation Delay



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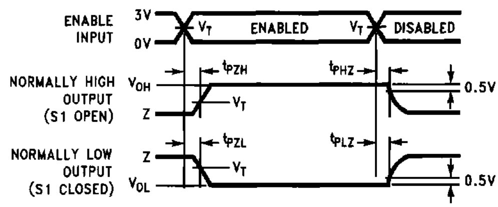
Enable and Disable



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Notes:

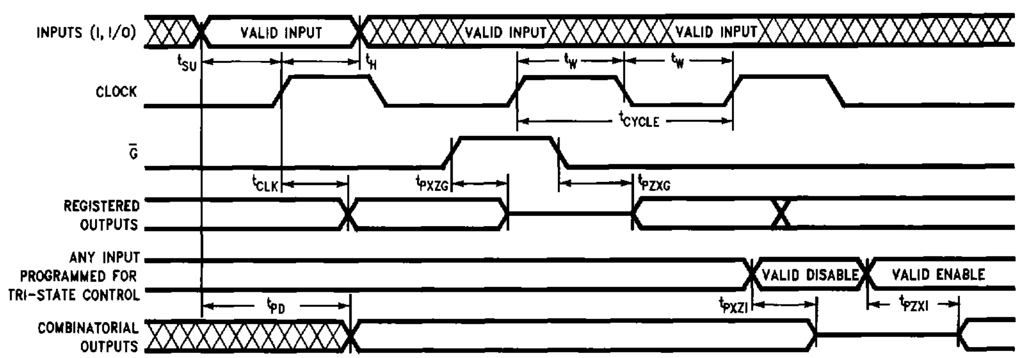
C_L includes probe and jig capacitance.

V_T = 1.5V.

Test inputs have rise and fall times of 3 ns between 0.3V and 2.7V.

In the example above, the phase relationships between inputs and outputs have been chosen arbitrarily.

Switching Waveforms



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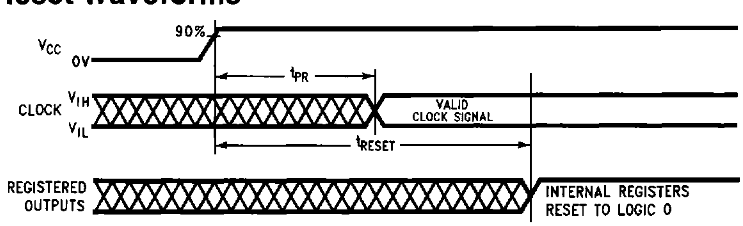
Power-Up Reset Waveforms



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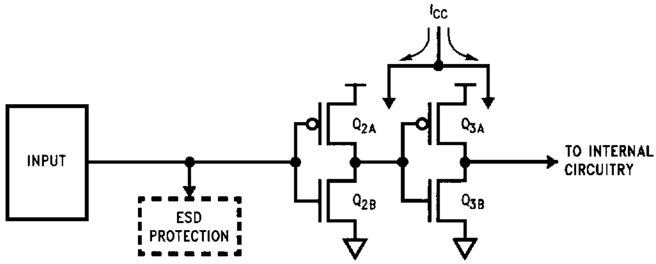
Input Schematic

Input Translator/Buffer



TL/L/11256-9

Functional Description

The GAL logic array consists of a programmable AND array with fixed OR-gate connections, similar to the bipolar PAL architecture. The logic array is organized as 20 complementary input lines crossing 64 "product term" lines with a programmable E²PROM cell at each intersection (2560 cells). Each programmable cell may establish a connection between an input line (true or complement phase of an array input signal) and a product term. A product term is satisfied (logically true) while all of the input lines "connected" to it are in the high logic state.

The 64 product terms are organized into eight output groups with eight terms each. Seven or eight of the product terms in each output group feed into an OR-gate to produce each output logic function; one of the product terms may instead be used to control the associated TRI-STATE device output. The fundamental transfer function of each GAL output is the familiar Boolean sum-of-products. Design development software is available which accepts Boolean equations and converts them automatically into GAL programming patterns.

As shown in the GAL20V8 Block Diagram *(Figure 1)*, a total of eight output logic functions are available. Each of the AND/OR logic functions feeds into an "output logic macrocell" (OLMC). The eight OLMCs control the flow of input and output signals between the logic array and the device's I/O pins.

Under control of an OLMC, each output may be designated either registered or combinatorial (non-registered). In the registered output configuration, the logic function output passes through a D-type flip-flop triggered by the rising edge of the clock input. Additionally, the logic function's output polarity may be designated active-low or active-high (adjusted before the register, if present). OLMC options such as these are selected using a set of programmable architecture control cells. These architecture cells are normally configured automatically by the development software or programming hardware.

All of the possible I/O configurations of the GAL20V8 are classified into three basic modes: "Small-PAL" mode, "Registered-PAL" mode and "Medium-PAL" mode. These modes correspond to the architectures of the PAL families which the GAL20V8 can emulate. The modes determine the mixture of OLMC configurations which can be selected for the device. The OLMC Selection table (Table I) lists which functions can be selected on device pins* 1, 13 and 15 through 22 for each of the three modes. The logic diagrams in *Figure 3* illustrate these OLMC functions.

"OUTPUT" represents the always-active combinatorial output configuration available in the "Small-PAL" mode. "REGISTER" is the registered output with register feedback available in the "Registered-PAL" mode. "I/O" is the combinatorial bidirectional I/O available in "Registered-PAL" and "Medium-PAL" modes. "TRI-STATE" is the TRI-STATE combinatorial output function appearing on pins* 15 and 22 in the "Medium-PAL" mode. "INPUT" in Table I denotes an OLMC used as a dedicated input only.

In the "Small-PAL" and "Medium-PAL" modes (Table I), pins* 1 and 13 are always dedicated inputs. In the "Registered-PAL" mode, however, pin* 1 becomes the clock input controlling all OLMC registers, and pin* 13 becomes the output enable ($\overline{G}$) input controlling the TRI-STATE outputs of all registered OLMCs. Within the "Small-PAL" and "Registered-PAL" modes in Table I, the functions of pins* 15 through 22 can be selected individually from either of the two functions listed. For example, in "Registered-PAL" mode, pins* 15 through 22 can each be designated as either a registered output or a combinatorial I/O. The "Medium-PAL" mode represents a single fixed configuration used to emulate combinatorial medium PAL devices (20L8, 20H8, 20P8).

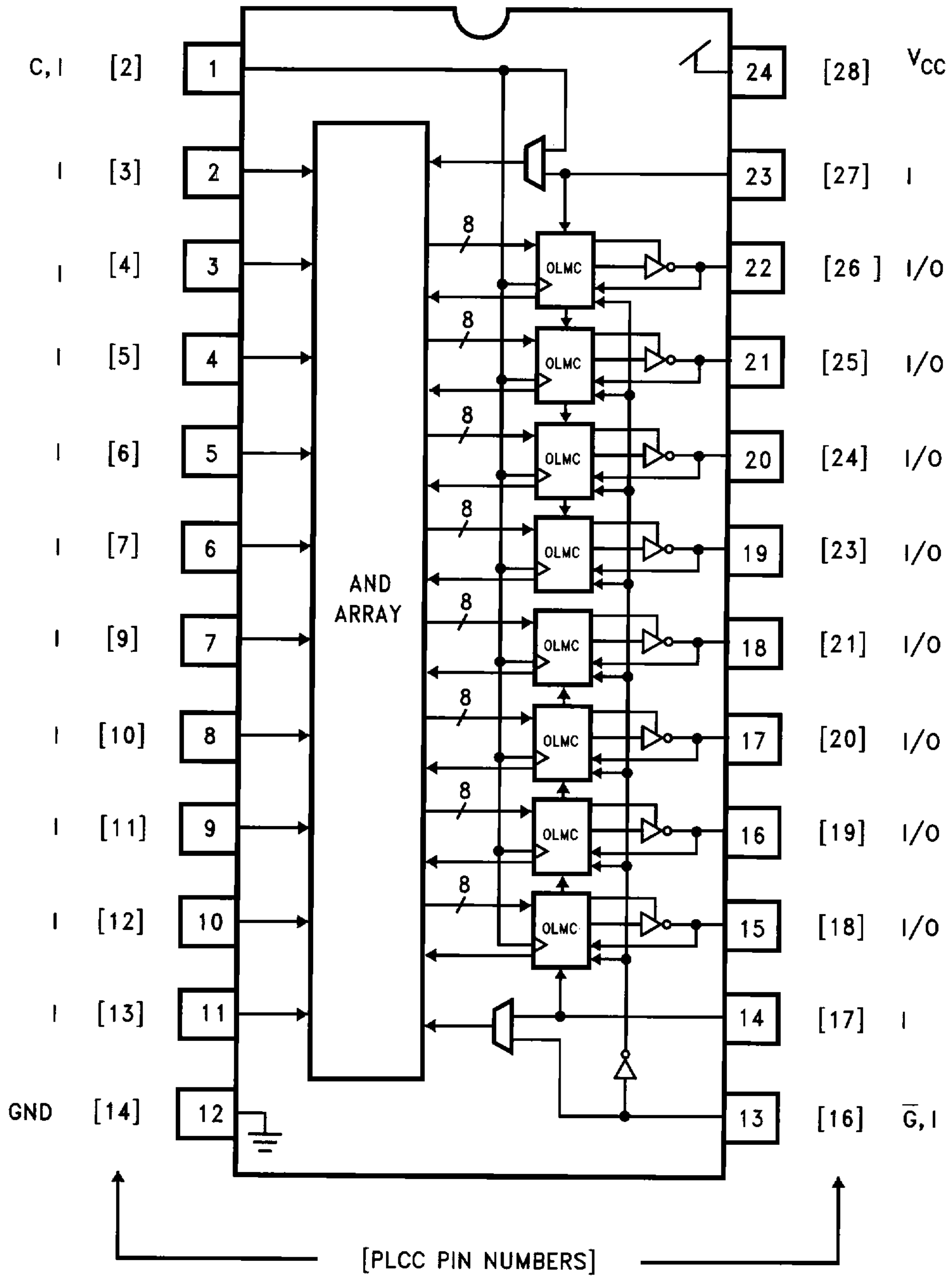
Table II lists the bipolar PAL products which the GAL20V8 can emulate, and the specific input/output configurations used. This is just a subset, however, of all the configurations provided in Table I.

All registers in a GAL device are reset to the low state upon power-up. The active-low outputs, in turn, assume high logic levels (if enabled) regardless of the selected output polarity. This may simplify sequential circuit design and test. To ensure successful power-up reset, V_{CC} must rise monotonically until the specified operating voltage is attained. During power-up, the clock input should assume a valid, stable logic state as early as possible (within the specified time, t_{PR}) to avoid interfering with the reset operation. The clock input should also remain stable until after the power-up reset operation is completed to allow the registers to capture the proper next state on the first high-going clock transition.

It should be noted that the switching of any input not logically connected to a product term or logic function has no effect on the associated output logic state. To minimize power consumption, however, unused inputs should be connected to a stable logic level such as ground or V_{CC} (CMOS GAL inputs may be tied directly to the supply voltage without causing excessive loading conditions).

*Applies to 24-pin DIP packages for GAL20V8; refer to the 28-lead PLCC Connection Diagram for conversion.

GAL20V8 Block Diagram—DIP Connections



TL/L/11256–10

FIGURE 1

28-Lead PLCC Connection Diagram

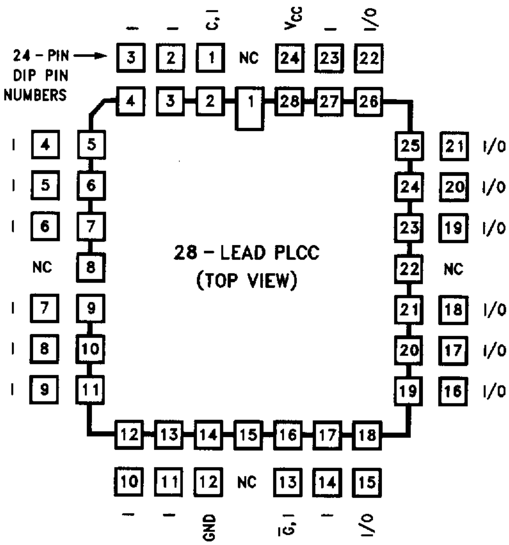


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FIGURE 2

Clock/Input Frequency Specifications

The clock frequency (f_{CLK}) parameter listed in the Recommended Operating Conditions table specifies the maximum speed at which the GAL registers are guaranteed to operate. Clock frequency is defined differently for the two cases in which register feedback is used versus when it is not. In a data-path type application, when the logic functions fed into the registers are not dependent on register feedback from the previous cycle (i.e., based only on external inputs), the minimum required cycle period (f_{CLK}^{-1} without feedback) is defined as the greater of the minimum clock period (t_w high + t_w low) and the minimum "data window" period (t_{SU} + t_H). This assumes optimal alignment between data inputs and the clock input. In sequential logic applications such as state machines, the minimum required cycle period ($t_{CYCLE} = f_{CLK}^{-1}$ with feedback) is defined as t_{CLK} + t_{SU}. This provides sufficient time for outputs from the registers to feed back through the logic array and set up on the inputs to the registers before the end of each cycle.

The input frequency (f_I) parameter specifies the maximum rate at which each GAL input can be toggled and still produce valid logic transitions on each combinatorial output. The f_I specification is derived as the inverse of the combinatorial propagation delay (t_{PD}).

Design Development Support

A variety of software tools and programming equipment is available to support the development of designs using GAL products. Typical software packages accept Boolean logic equations to define desired functions. Most are available to run on personal computers and generate a JEDEC-compatible "cell-map" (analogous to a PAL "fuse-map"). The industry-standard JEDEC format ensures that the resulting cell-map file can be down-loaded into a variety of programming equipment. Many software packages and programming units support a large variety of programmable logic products as well. The OPAL software package from National Semiconductor supports all programmable logic products available from National and is fully JEDEC-compatible.

National strongly recommends using only approved programming hardware and software for developing GAL designs. Programming using unapproved equipment generally voids all guarantees. Approved programmers incorporate specialized programming algorithms that program the array and automatically configure the architecture cells. To ensure data retention and reliability, the programming algorithm also tracks the number of programming cycles to which each GAL device has been subjected since shipment, and stores this information automatically in the device.

Design Development Support (Continued)

The special GAL programming algorithm can also program a GAL device using a standard fuse-map developed for any of the emulated PAL products. PAL fuse-maps can be created by any JEDEC-compatible PAL development software or by loading the fuse pattern from an existing programmed PAL device into the programming unit (provided the PAL device has not been secured). However, to utilize the full flexibility of the GAL architecture, true GAL development software (such as OPAL software) is recommended.

Detailed logic diagrams showing all JEDEC cell-map addresses in the GAL logic array and OLMC are provided for direct map editing and diagnostic purposes (see "Programming Details"). For a list of current software and programming support tools available for these devices, please contact your local National sales representative or distributor. If detailed specifications of the GAL programming algorithm are needed, please contact the National Semiconductor Programmable Device Support department.

OLMC Selection Table

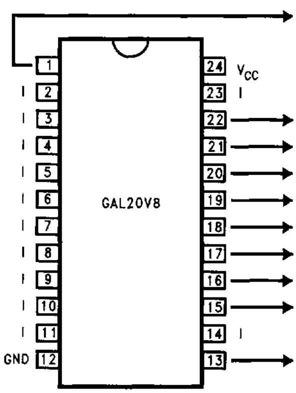

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TABLE I

"Small-PAL" Mode	"Registered-PAL" Mode	"Medium-PAL" Mode
INPUT	CLOCK	INPUT
INPUT or OUTPUT*	REGISTER or I/O	TRI-STATE**
INPUT or OUTPUT*	REGISTER or I/O	I/O
INPUT or OUTPUT*	REGISTER or I/O	I/O
OUTPUT*	REGISTER or I/O	I/O
OUTPUT*	REGISTER or I/O	I/O
INPUT or OUTPUT*	REGISTER or I/O	I/O
INPUT or OUTPUT*	REGISTER or I/O	I/O
INPUT or OUTPUT*	REGISTER or I/O	TRI-STATE**
INPUT	OUTPUT ENABLE ($\overline{G}$)	INPUT

*Active combinatorial output

**TRI-STATE combinatorial output

Note: Pin numbers above apply to 24-pin DIP packages; refer to the 28-lead PCC Connection Diagram for conversion.

PAL Replacement Configurations

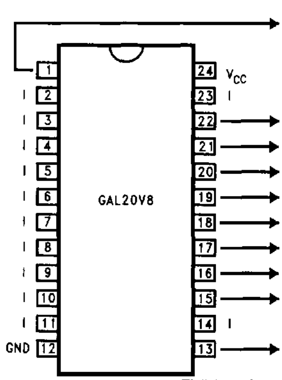

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TABLE II

	"Small-PAL" Mode				"Registered-PAL" Mode			"Medium-PAL" Mode
	INPUT	INPUT	INPUT	INPUT	CLOCK	CLOCK	CLOCK	INPUT
	OUTPUT*	INPUT	INPUT	INPUT	REGISTER	I/O	I/O	TRI-STATE**
	OUTPUT*	OUTPUT*	INPUT	INPUT	REGISTER	REGISTER	I/O	I/O
	OUTPUT*	OUTPUT*	OUTPUT*	INPUT	REGISTER	REGISTER	REGISTER	I/O
	OUTPUT*	OUTPUT*	OUTPUT*	OUTPUT*	REGISTER	REGISTER	REGISTER	I/O
	OUTPUT*	OUTPUT*	OUTPUT*	OUTPUT*	REGISTER	REGISTER	REGISTER	I/O
	OUTPUT*	OUTPUT*	OUTPUT*	INPUT	REGISTER	REGISTER	REGISTER	I/O
	OUTPUT*	OUTPUT*	INPUT	INPUT	REGISTER	REGISTER	I/O	I/O
	OUTPUT*	INPUT	INPUT	INPUT	REGISTER	I/O	I/O	TRI-STATE**
	INPUT	INPUT	INPUT	INPUT	$\overline{G}$	$\overline{G}$	$\overline{G}$	INPUT
Emulated PAL Products	14L8 14H8 14P8	16L6 16H6 16P6	18L4 18H4 18P4	20L2 20H2 20P2	20R8 20RP8	20R6 20RP6	20R4 20RP4	20L8 20H8 20P8

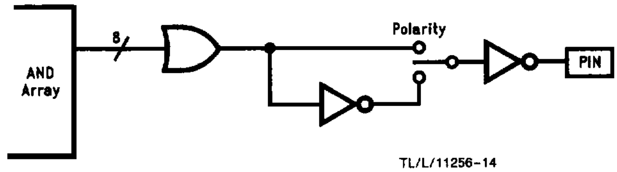
* Active combinatorial output.

**TRI-STATE combinatorial output.

Note: Pin numbers above apply to 24-pin DIP packages; refer to the 28-pin PCC Connection Diagram for conversion.

OLMC Configurations

OUTPUT (Active Combinatorial Output)



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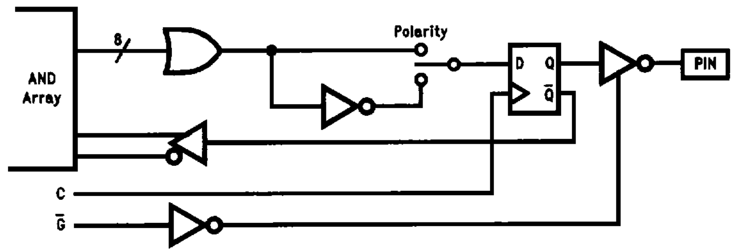
REGISTER (Registered Output)



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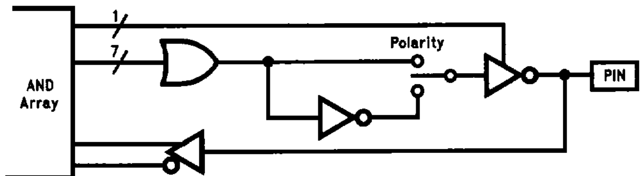
I/O (Combinatorial Input/Output)



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TRI-STATE (TRI-STATE Combinatorial Output)

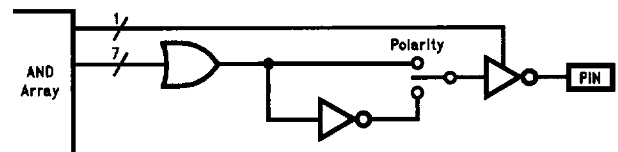

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FIGURE 3

Security Cell

A security cell is provided on all GAL20V8 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, the circuitry enabling array access is disabled, preventing further programming or verification of the array. The security cell can be erased only in conjunction with the array during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed.

Electronic Signature

Each GAL device contains an electronic signature word consisting of 64 bits of reprogrammable memory. The electronic signature word can be programmed to contain any identification information desired by the user. Some uses include pattern identification labels, revision numbers, dates, inventory control information, etc. The data stored in the electronic signature word has no effect on the functionality of the device. The information is read out of the device using the normal program verification procedure provided by the programming equipment. The information may be accessed at any time independent of the state of the security cell. National's OPAL development software allows electronic signature data to be entered by the user and downloaded to the programming equipment.

Bulk Erase

The programming equipment automatically performs a bulk erase operation prior to each programming operation. No special erase operation need be performed by the user. Bulk erase clears the logic array, architecture cells, security cell, and electronic signature information. The GAL device is thereby reverted back to its virgin state.

Latch-Up Protection

GAL devices are designed with an on-chip charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

To insure that no undesired bias conditions occur with P+ diffusions, a Latch-Lock™ power-up circuitry has been developed. The drain of all P channel devices normally connected to the device supply are now connected to an alternate supply that powers up after the device N-wells have been biased and the substrate has reached its negative clamp value. This prevents any hazardous bias conditions from developing in the power-up sequence. After power-up is complete, the Latch-Lock circuitry becomes dormant until a full power-down has occurred; this eliminates the chance of an unwanted P channel power-down during device operation.

Manufacturer Testing

Because of EECMOS technology, GAL devices can be reprogrammed in milliseconds. This allows each device to be completely tested by the manufacturer using numerous logic array and architecture patterns prior to shipping. Every programmable cell and every logic path through every device is fully tested for programmability, functionality and performance to all AC and DC parameters. The customer can therefore expect 100% programming and functional yield and 100% compliance of all GAL products to datasheet specifications.

The testing procedure performed on all GAL devices by the manufacturer tests all aspects of device operation. Extensive testing of all programmable cells in the device include margin testing, internal verify, and program retention during high-temperature bake. All DC and AC parameters are tested at hot and cold temperatures using a variety of worst-case logic and signal patterns. Functional tests include reprogramming each OLMC to all valid architectural configurations.

Register Preload

The register preload feature allows OLMC registers to be directly loaded with any desired data pattern. It also allows the present state of OLMC registers to be examined regardless of TRI-STATE control conditions. This simplifies testing of devices after programming. A device may be put into any desired register state at any point during the functional test sequence. The test sequence may then be resumed to verify proper next-state transitions. This allows complete verification of sequential logic circuits, including states that are normally impossible or difficult to reach. It may also shorten the overall test time significantly.

Register preload is not an operational mode and is not intended for board-level testing because elevated voltage levels must be applied to the device. The programming equipment normally provides the register preload capability as part of its functional test facility. Note that the testing of GAL devices after programming by the user may be considered unnecessary because all EECMOS GAL products are completely tested by the manufacturer, guaranteeing 100% post-programming functional yield.

The register preload algorithm is described for those users who wish to test programmed GAL devices using test equipment other than approved GAL programming equipment. As shown in the Register Preload Waveform in *Figure 5*, the preload sequence must not begin until the normal power-up reset operation has completed (after time t_{RESET}). The device is placed into preload mode by raising the "PRLD" input (pin* 13) to voltage V_{IES}, as specified in the Register Preload Specifications (Table III).

To preload the OLMC registers, a series of data bits are shifted into the device on the "S_{DIN}" input (pin* 11), one bit for each OLMC in which registered output has been selected. (Non-registered OLMCs are bypassed.) The shift sequence is clocked by the rising edge of the "D_{CLK}" input (pin* 1). The data stream is shifted in through the registered OLMC with the lowest corresponding pin number, and then "upward" through all remaining registered OLMCs in pin-number ascending order. Therefore, the first data bit in the series is ultimately loaded into the registered OLMC with the highest corresponding pin number, as shown in *Figure 4*.

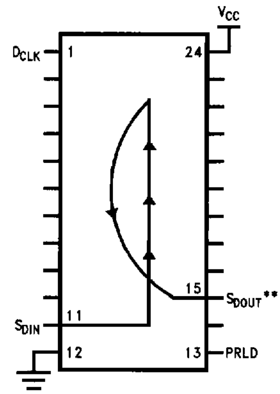
*Applies to 24-pin DIP packages for GAL20V8; refer to the 28-lead PLCC Connection Diagram for conversion.

Register Preload (Continued)

As the data series is shifted into the S_{DIN} input, the contents of all registers (in registered OLMCs) are shifted "upward" and out onto the "S_{DOUT}" output (pin* 15). Complete present-state information can be examined in this manner. Test fixtures can be devised to test several GAL devices in which the S_{DOUT} pin of each chip is connected to the S_{DIN} pin of the next, and all preload and present-state data can be shifted around a single serial loop.

Note that when shifting register data into S_{DIN} or out of S_{DOUT}, V_{IL}/V_{OL} = register reset (0), and V_{IH}/V_{OH} = register set (1). These 0 and 1 register states are always inverted (active-low) on the normal output pins regardless of the selected output polarity (polarity affects logic function values before register inputs).

*Applies to 24-pin DIP packages for GAL20V8; refer to the 28-lead PLCC Connection Diagram for conversion.



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**The S_{DOUT} output buffer is an open drain output during preload. This pin should be terminated to V_{CC} with a 10 kΩ resistor.

FIGURE 4. Output Register Preload Pinout

Register Preload Specifications

TABLE III

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input Voltage (High)		2.40		V_{CC}	V
V_{IL}	Input Voltage (Low)		0.00		0.50	V
V_{IES}	Register Preload Input Voltage		11.5	12	12.5	V
V_{OH}	Output Voltage (High) (Note 1)				V_{CC}	V
V_{OL}	Output Voltage (Low) (Note 1)	$I_{OL} \leq 12$ mA	0.00		0.50	V
I_{IH}, I_{IL}	Input Current (Programming)			±1	±10	μA
I_{OH}	High Level Output Current (Note 1)	$V_{OH} \leq V_{CC}$			10	μA
t_{PWV}	Verify Pulse Width		1	5	10	μs
t_D	Pulse Sequence Delay		1	5	10	μs
t_{RESET}	Register Reset Time from Valid V_{CC}				45	μs

Note 1: The S_{DOUT} output buffer is an open drain output. This pin should be terminated to V_{CC} with a 10k resistor.

Register Preload Waveforms

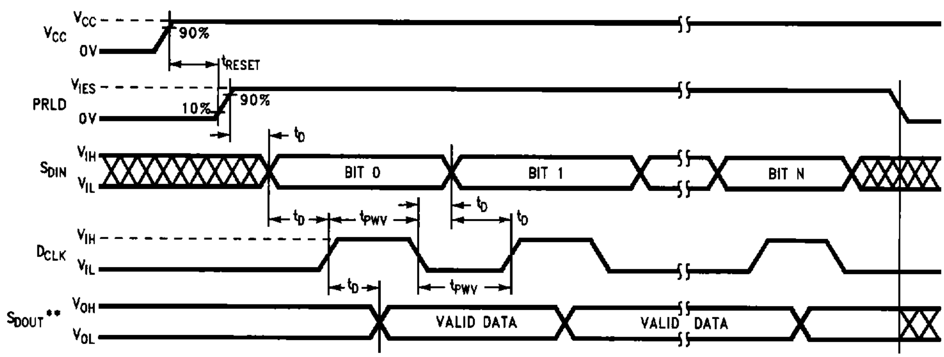

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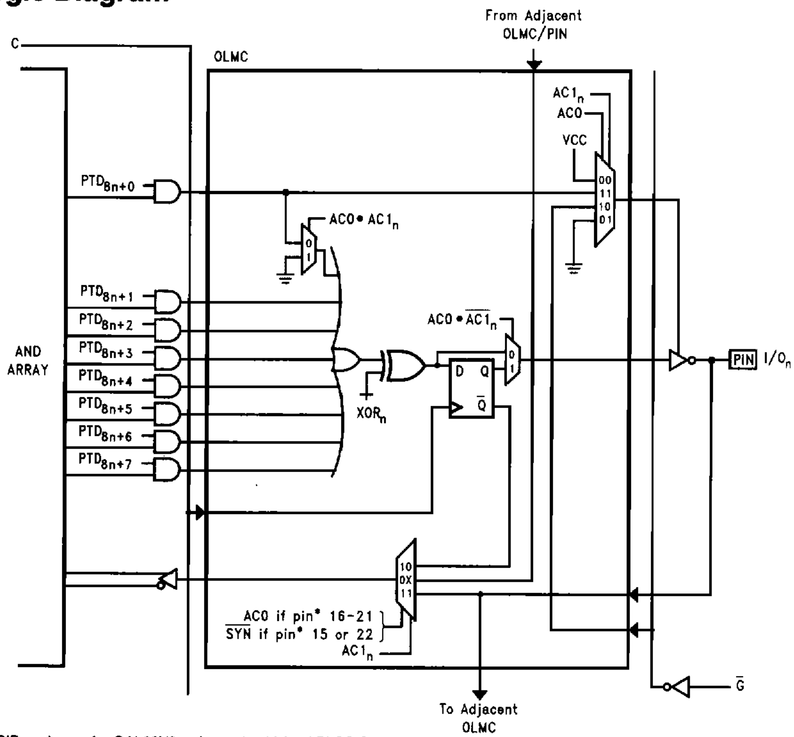
FIGURE 5

**The S_{DOUT} output buffer is an open drain output during preload. This pin should be terminated to V_{CC} with a 10 kΩ resistor.

OLMC Logic Diagram



*Applies to 24-pin DIP packages for GAL20V8; refer to the 28-lead PLCC Connection Diagram for conversion.

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FIGURE 6

OLMC Architecture Programming

TABLE IV

	"Small-PAL" Mode			"Registered-PAL" Mode			"Medium-PAL" Mode	
	Function		JEDEC Input Line #s (Note 1)	Function		JEDEC Input Line #s (Note 1)	Function	JEDEC Input Line #s (Note 1)
Pin 1	INPUT	INPUT	2, 3	CLOCK	CLOCK		INPUT	2, 3
Pin 23	INPUT	INPUT	6, 7	INPUT	INPUT	2, 3	INPUT	6, 7
***Pin 22	I/O	INPUT	10, 11	REGISTER	I/O	6, 7	TRI-STATE**	
***Pin 21	I/O	INPUT	14, 15	REGISTER	I/O	10, 11	I/O	10, 11
***Pin 20	I/O	INPUT	18, 19	REGISTER	I/O	14, 15	I/O	14, 15
***Pin 19	OUTPUT*	NC		REGISTER	I/O	18, 19	I/O	18, 19
***Pin 18	OUTPUT*	NC		REGISTER	I/O	22, 23	I/O	22, 23
***Pin 17	I/O	INPUT	22, 23	REGISTER	I/O	26, 27	I/O	26, 27
***Pin 16	I/O	INPUT	26, 27	REGISTER	I/O	30, 31	I/O	30, 31
***Pin 15	I/O	INPUT	30, 31	REGISTER	I/O	34, 35	TRI-STATE**	
Pin 14	INPUT	INPUT	34, 35	INPUT	INPUT	38, 39	INPUT	34, 35
Pin 13	INPUT	INPUT	38, 39	G̅	G̅		INPUT	38, 39
	$AC1_n = 0$	$AC1_n = 1$		$AC1_n = 0$	$AC1_n = 1$		$AC1_n = 1$	
	SYN = 1, AC0 = 0			SYN = 0, AC0 = 1			SYN = 1, AC0 = 1	
	All outputs are combinatorial and always active.			At least one output is registered.			All I/O pins are combinatorial.	

Note: Pin numbers above apply to 24-pin DIP packages; refer to the 28-lead PLCC Connection Diagram for conversion.

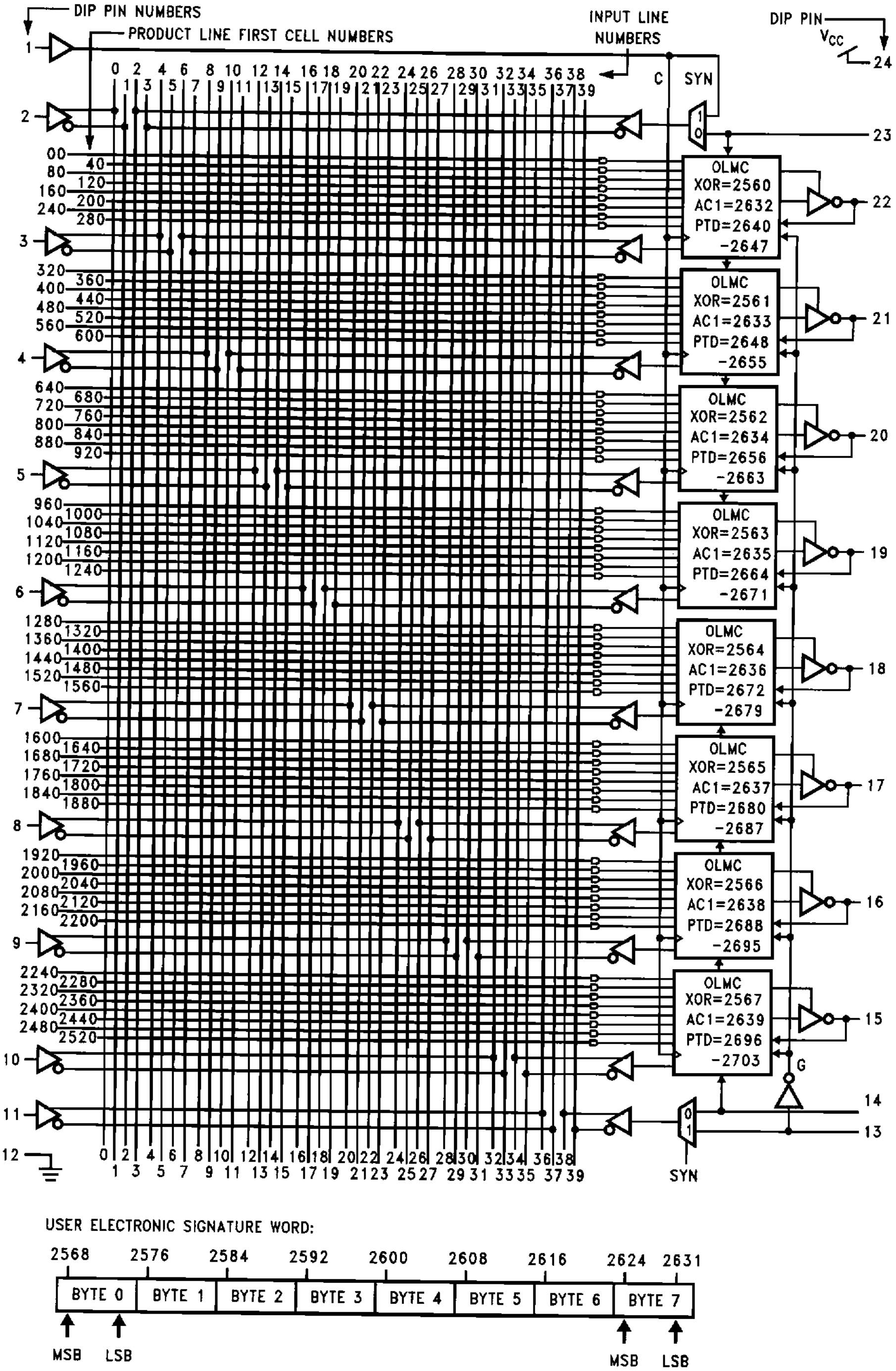
Note 1: All even and odd numbered JEDEC input line numbers correspond to true and complement array inputs, respectively.

*Active combinatorial output.

**TRI-STATE combinatorial output.

***$AC1_n$ applies to these I/O pins only.

GAL20V8 Logic Diagram



SYN=2704
AC0=2705

JEDEC Logic Array Cell Number = Product Line First Cell Number + Input Line Number

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FIGURE 7

Programming Details

Understanding the information in this section is not essential when using approved programming equipment and software for developing GAL designs. This is a more thorough disclosure of the GAL architecture provided for direct JEDEC cell-map editing and diagnostic purposes. This section alone, however, does not contain sufficient information to implement the GAL programming algorithm. If detailed specifications of the GAL programming algorithm are needed, please contact the National Semiconductor Programmable Device Support department.

As mentioned in the Functional Description, the OLMC is responsible for selecting input and/or output paths, registered vs. combinatorial outputs, active-high or low polarity, and common vs. locally-controlled TRI-STATE control. Additionally, the OLMCs select between alternate logic array input paths to maintain JEDEC cell-map compatibility with either "small-PAL" or "medium-PAL" logic arrays.

The various configurations of the OLMCs are controlled by a set of programmable "architecture" cells, separate from the logic-defining array cells. Each GAL device contains two "global" architecture cells, "SYN" and "AC0", which affect all OLMCs. Each of the devices's eight OLMCs also contains two "local" cells, "AC1" and "XOR". The OLMC Logic Diagram in *Figure 6* shows how the architecture cells select the different paths through the OLMC.

The SYN bit controls whether a device will have any registered outputs (SYN = 0) or will be purely combinatorial (SYN = 1). The SYN bit determines whether device pins* 1 and 13 are used as the clock and global TRI-STATE control inputs (SYN = 0) or whether they are ordinary inputs (SYN = 1). The AC0 bit selects between the "Small-PAL" mode and the "Medium/Registered-PAL" modes. The function of the AC1 bits depend on the state of the AC0 bit. In "Small-PAL" mode (AC0 = 0), the AC1 bit in each OLMC determines whether the associated device pin is an output (AC1 = 0) or an input (AC1 = 1). In "Registered-PAL" mode (AC0 = 1), the AC1 bit determines whether each OLMC is registered (AC1 = 0) or combinatorial (AC1 = 1). In "Medium-PAL" mode (AC0 = 1), the AC1 bits in all OLMCs must be set to 1 (combinatorial). All of the valid architecture bit configurations are shown in the OLMC Architecture table (Table IV), which has the same familiar format used in the OLMC Selection table (Table I).

Independent of SYN, AC0 and the AC1 bits, the XOR bit in each OLMC selects between active-low (XOR = 0) or active-high (XOR = 1) output polarity.

*Applies to 24-pin DIP packages for GAL20V8; refer to the 28-lead PLCC Connection Diagram for conversion.

Ordering Information

GAL 20 V 8 A -15 L N C

- GAL — Generic Array Logic Family
- 20 — Number of Array Inputs
- V — Output Type:
  V = Variable Architecture
- 8 — Number of Outputs
- A — -12/-15 Only
- -15 — Speed:
  -7: t_{PD} = 7.5 ns
  -10: t_{PD} = 10 ns
  -12: t_{PD} = 12 ns
  -15: t_{PD} = 15 ns
  -20: t_{PD} = 20 ns
  -25: t_{PD} = 25 ns
- L — L = Low Power
  Q = Quarter Power
- N — Package Type:
  N = 24-Pin Plastic DIP
  V = 28-Lead Plastic Chip Carrier
- C — Temperature Range:
  C = Commercial (0°C to +75°C)
  I = Industrial (−40°C to +85°C)

THE GAL20V8A-10L HAS BEEN RENAMED GAL20V8-10L.
THERE WERE NO SPECIFICATION CHANGES ASSOCIATED WITH THIS NAME CHANGE.