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SERVICE MANUAL

**A500 PLUS
INCLUDES A501 PLUS
RAM EXPANDER**

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TABLE OF CONTENTS

SECTION 1 — SPECIFICATIONS

A500 PLUS SPECIFICATIONS..... 1-1
 A501 PLUS SPECIFICATIONS..... 1-2

SECTION 2 — THEORY OF OPERATIONS

AMIGA 500 PLUS MEMORY MAP..... 2-1
 A500 PLUS BLOCK DIAGRAM..... 2-2
 THEORY OF OPERATION..... 2-3
 8375 AGNUS 2MEG..... 2-7
 8373 DENISE HI RES..... 2-11
 8364 PAULA..... 2-12
 GARY..... 2-13

SECTION 3 — TROUBLESHOOTING

MAIN ASSEMBLY DIAGRAM..... 3-1

SECTION 4 — PARTS

A500 PLUS PCB ASSEMBLY 312812..... 4-1
 A500 PLUS SHIPPING ASSEMBLIES..... 4-2
 A500 PLUS MAJOR ASSEMBLIES..... 4-3
 A500 PLUS PCB COMPONENTS..... 4-4
 A501 PLUS SHIPPING ASSEMBLIES..... 4-5
 A501 PLUS MAJOR ASSEMBLIES..... 4-6
 A501 PLUS PCB COMPONENTS..... 4-7

SECTION 5 — SCHEMATICS

A500 PLUS SCHEMATIC #312813, REV. 1..... 5-1
 A501 PLUS SCHEMATIC #363835, REV. 0..... 5-11

A500 PLUS SPECIFICATIONS

INTRODUCTION

The A500 Plus is a feature enhanced version of the A500 personal computer.

FEATURES

CPU: 7.16 MHz 68000 NTSC; 7.09 MHz 68000 PAL

Memory: 1 Megabyte standard expandable to 2 MB with addition of A501 Plus

Kickstart ROM: 512K (V2.04)

Mass Storage Memory: Internal, 3.5 inch FDD mounted on the right side, the same as the A500.

Additional Features: Real Time Clock (on-board) with battery backup.

APPEARANCE

The A500 Plus appearance shall be the same as the A500. A new logo plate has been added to distinguish "A500" from "A500 Plus". The color is the same light beige as the current A500.

WHAT'S ADDED

1 Meg on-board memory expandable to 2 Meg.

8375 FAT AGNUS which supports 2 Meg. of Chip RAM

On-board Real Time Clock

8373 ECS Denise

Full ECS support

V2.04 in ROM

CUSTOM CHIPS

The A500 Plus shall contain the same custom chip set as the A500, except for the 8375 2Meg. FAT AGNUS and 8373 ECS Denise.

SYSTEM I/O

EXTERNAL SYSTEM I/O

External floppy, Serial, Parallel, Mouse, Joystick, Stereo Audio Ports

These Ports remain unchanged from their A500 counterparts.

MEMORY MAP

The A500 Plus Memory Map is the same as the A500 Memory Map.

A501 PLUS SPECIFICATIONS

DESCRIPTION

The A501 Plus is a memory expansion board for the Amiga 500 Plus personal computer. It has 1 MB of "chip" memory and interfaces directly to the A500 Plus memory expansion slot. Unlike the A501, the A501 Plus doesn't have a Real Time Clock (RTC), the A500 Plus has a built-in RTC.

The A501 can be used in either the A500 or A500 Plus personal computer, has 512K of memory and includes a Real Time Clock. The A500 maps the A501 into pseudo-fast memory while the A500 Plus maps it into chip memory. In addition, when used in an A500 Plus system, the internal (built-in) RTC is selected.

Both the A501 and A501 Plus uses the same printed circuit board (PCB). In the A501 Plus, the RTC and refresh feature components are not loaded.

MEMORY TYPE

The A501 Plus shall use 256K x 4 120ns DRAMs.

PIN DESCRIPTIONS

<i>PIN NAME</i>	<i>PIN NUMBER</i>	<i>SIGNAL DIRECTION</i>	<i>DESCRIPTION</i>
+5	1-2, 51-52	I	+ 5 Volts
GND	3-4, 21-22, 53-54		Signal Ground
XDRD (0-15)	5-20	I/O	Memory Data Bus
XDRA (0-8)	23-31	I	Memory Address Bus
/EXTICK	32	O	Active low. When this signal is asserted, it allows the A500 to detect the presence of an A501. The A501 Plus does not use this signal.
/XCLKS	33	I	Active low. When this signal is asserted, the external RTC is selected. This signal is not used in the A501 Plus.
/XOE	34	I	Active low. When this signal is asserted, data can be read from the expansion memory.
/XCASL	35	I	Active low. This signal strobes the column address into DRAMs and corresponds to the low byte of the data word.
/XCASU	36	I	Active low. This signal strobes the column address into the DRAMs and corresponds to the high byte of the data word.
/XRAS1	37	I	Active low. This signal strobes the row address into the DRAMs and corresponds to the upper 512K of the expansion RAM.
/XRAS0	38	I	Active low. This signal strobes the row address into the DRAMs and corresponds to the lower 512K of the expansion RAM.
/XWE	39	I	Active low. When this signal is asserted, data is written into the expansion memory.
NC	40, 56		Not connected.
XD (0-3)	41-44	I/O	RTC Data bus. These lines are not used in the A501 Plus.
XA (2-5)	45-48	I	RTC Address Bus. These lines are not used in the A501 Plus.
/XCLKRD	49	I	Active low. When this signal is asserted, data can be read from the RTC. This signal is not used in the A501 Plus.
/XCLKWR	50	I	Active low. This signal strobes the data and address into the RTC. This signal is not used in the A501 Plus.
+12V	55	I	+ 12 Volts. This is used on the A501 to charge the battery. This line is not used on the A501 Plus.

A501 PLUS SPECIFICATIONS (Continued)

FACTORY DEFAULT JUMPER SETTINGS

	JP1	JP2A	JP2B	JP3	JP9
A501	1-2 shorted	1-2 open 2-3 shorted	1-2 open 2-3 shorted	1-2 shorted 1-2 shorted 1-1 open 2-2 open	1-2 open
A501 Plus	1-2 shorted	1-2 shorted 2-3 open	1-2 shorted 2-3 open	1-2 shorted 1-2 shorted 1-1 open 2-2 open	1-2 open

Jumper

Function

- JP1** When 1-2 are shorted, /EXTICK detection is enabled. This jumper has no effect on the A501 Plus, because it does not use /EXTICK detection.
- JP2A, JP2B** When 2-3 are shorted (1-2 open), it enables the refresh feature in the A501. Refresh components U11-U13 must be loaded in the A501. The refresh feature is only required on the A501 to compensate for refresh deficiencies in older revs of the A500.
- JP3** Swaps upper and lower bank DRAMs. When 1-2 are shorted (1-1 and 2-2 open), /XRAS0 and /XRAS1 selects the lower and upper banks respectively. Conversely, when 1-1 and 2-2 are shorted, /XRAS0 selects the upper bank while /XRAS1 selects the lower bank RAMs.
- JP9** Overwrites /XCLKS. When 1-2 are shorted, /XCLKS is permanently enabled and the A501 (external) RTC is always selected. This jumper is normally open. Selection of internal or external RTC is done by the A500 or A500 Plus via the /XCLKS line. RTC components U9, U11-U13, C9, C11-C13, C911, C913, R911-R915, D11-D9123, BT9, TC9 and Y9 must be loaded in the A501.

DIMENSIONS

- Length: 5.5 in.
- Width: 3.5 in.

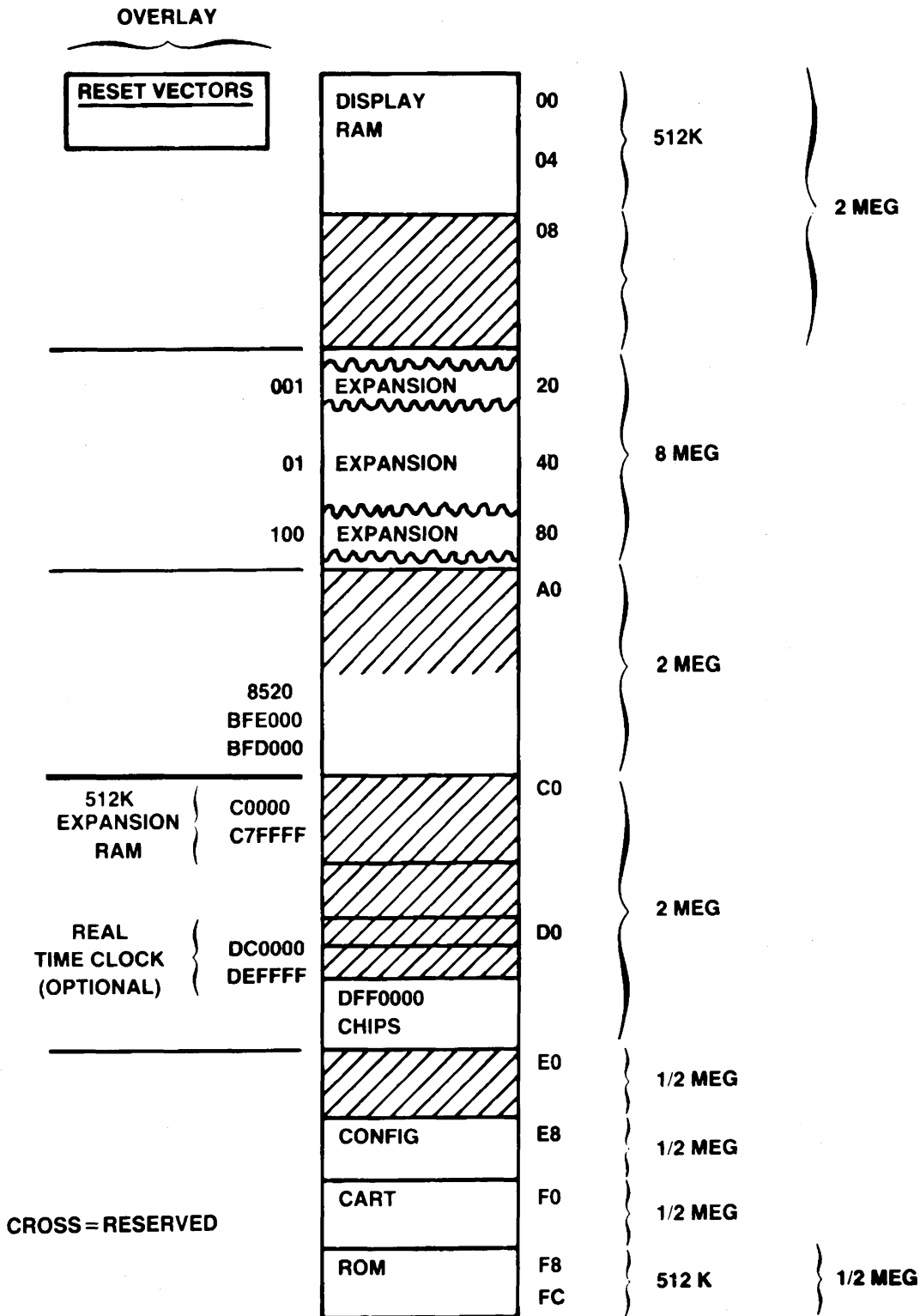
POWER

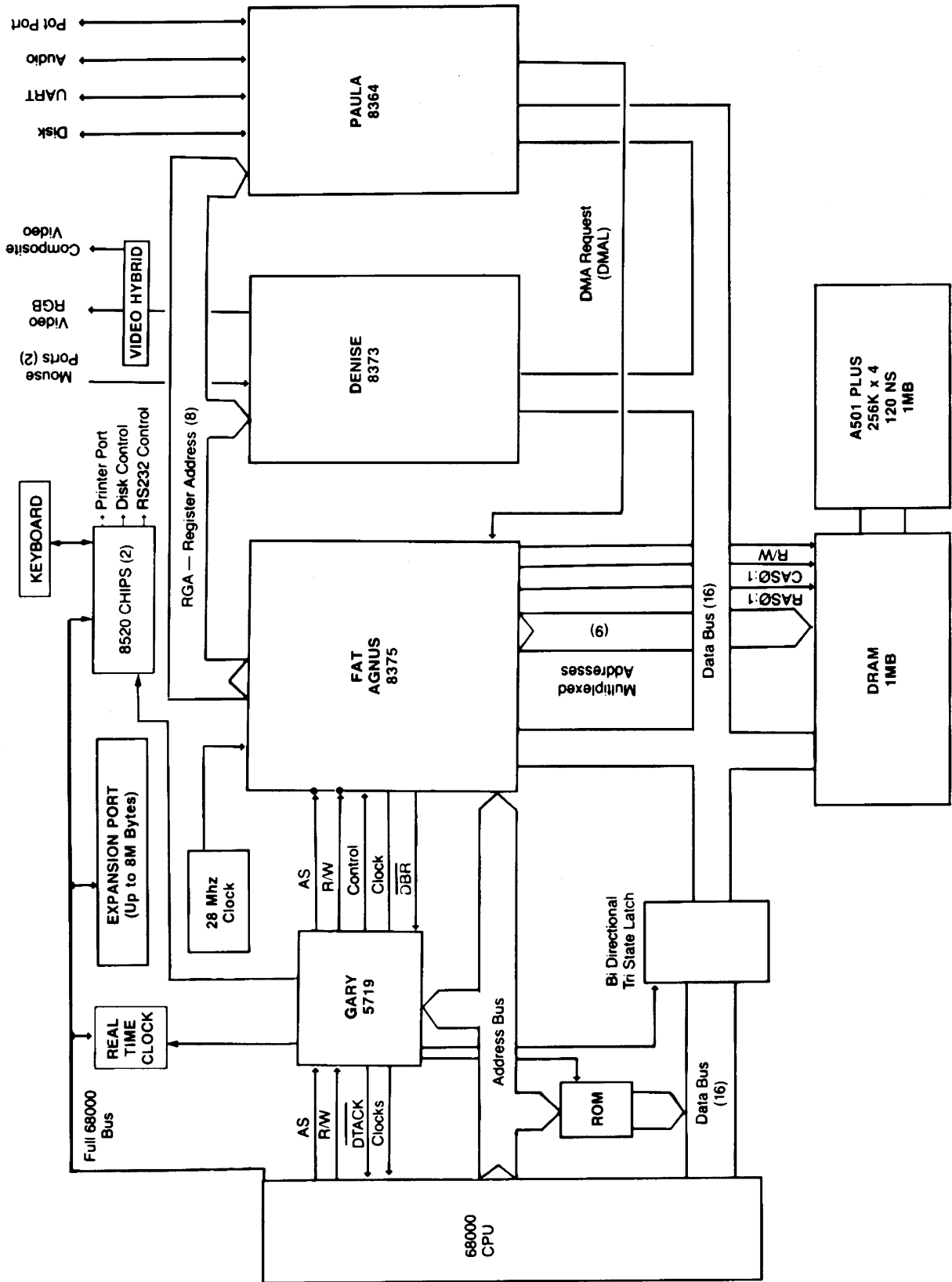
- +5VDC @330 mA MAX for A501 Plus
@280 mA MAX for A501
- +12VDC @15 mA MAX for A501
Not Used on A501 Plus

ENVIRONMENT

- Operating Temperature 0 to +55°C
- Humidity Up to 90% without condensation

AMIGA 500 PLUS MEMORY MAP





A500 PLUS BLOCK DIAGRAM

THEORY OF OPERATION

The AMIGA 500 Plus computer is a high-performance system with advanced graphics and audio features. The principal hardware features consist of the 68000 microprocessor which runs at 7.2 MHz, 1MB RAM, expandable to 2MB, and configurable to 8MB, 2 parallel I/O chips, one control chip (GARY) and 3 custom VLSI chips that provide the unique capabilities for animation, graphics and sound.

68000 MICROPROCESSOR

The 68000 is the CPU of the system. All other resources are under software control via control data issued from it. All 3 custom chips have control registers that are written by the 68000.

The 68000 communicates with the rest of the computer via its address bus, data bus and control lines. Notice that in the block diagram the 3 custom chips do not reside directly on the 68000 buses. When the 68000 starts a bus cycle that is intended for the custom chips or the display RAM, the bus control chip detects whether or not the display RAM buses are available. The control chip will not assert the acknowledge signal (/DTACK) back to the 68000 until the display RAM buses are available. Once the 68000 receives /DTACK it completes the bus cycle. Connecting the display RAM buses to the 68000 buses is discussed further in the section on bus control. Because the display RAM is capable of approximately twice the bandwidth of the 68000, the 68000 is usually not delayed by waiting for the display buses to become available.

The 68000 can fetch instructions from:

- Display RAM
- ROM

The 68000 can read and write data directly to:

- Display RAM
- Parallel I/O Chips
- 3 Custom I.C.s
- ROM

The 68000 transmits data and control to and from the peripherals via the parallel I/O and the 3 custom chips.

7M is the processor clock to the 68000. C1, C3 and CDAC are used to clock the custom chips and determine the timing of signals to the memory arrays.

ROM

The ROM contains the kernel and DOS routines; it is 128K × 16.

PARALLEL I/O

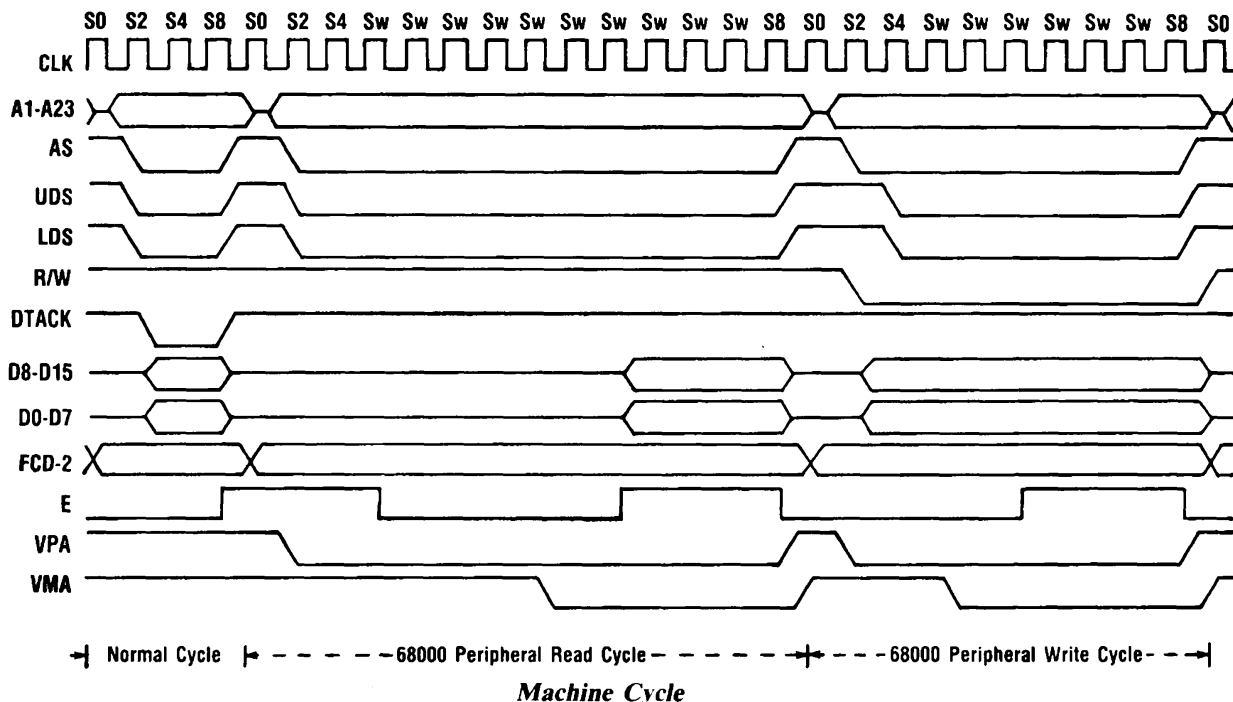
The 2 multipurpose 8520 I/O chips provide the following:

- I/O to and from the parallel port connector
- Control lines to and from the joystick/mouse ports
- A control line to the front panel LED
- Internal control lines
- Keyboard control lines, clock and data
- Serial port control lines
- Floppy disk interface control lines
- Internal timers

These 2 chips reside on the 68000 buses and are read and written by the 68000.

THEORY OF OPERATION (Continued)

CPU SIGNAL SUMMARY



Signal Name	Mnemonic	Input/Output	Active State	Three State
Address Bus	A1-A23	Output	High	Yes
Data Bus	D0-D15	Input/Output	High	Yes
Address Strobe	\overline{AS}	Output	Low	Yes
Read/Write	R/\overline{W}	Output	Read-High Write-Low	Yes
Upper and Lower Data Strobes	$\overline{UDS}, \overline{LDS}$	Output	Low	Yes
Data Transfer Acknowledge	\overline{DTACK}	Input	Low	No
Bus Request	\overline{BR}	Input	Low	No
Bus Grant	\overline{BG}	Output	Low	No
Bus Grant Acknowledge	\overline{BGACK}	Input	Low	No
Interrupt Priority Level	$\overline{IPL0}, \overline{IPL1}, \overline{IPL2}$	Input	Low	No
Bus Error	\overline{BERR}	Input	Low	No
Reset	\overline{RESET}	Input/Output	Low	No*
Halt	\overline{HALT}	Input/Output	Low	No*
Enable	E	Output	High	No
Valid Memory Address	\overline{VMA}	Output	Low	Yes
Valid Peripheral Address	\overline{VPA}	Input	Low	No
Function Code Output	FC0, FC1, FC2	Output	High	Yes
Clock	CLK	Input	High	No
Power Input	Vcc	Input	—	—
Ground	GND	Input	—	—

*Open Drain
A0 is internal to 68000

THEORY OF OPERATION (Continued)

CLOCKS GENERATOR

The entire computer board is run synchronously to the 3.57954Mhz color clock (C1). This is accomplished by generating a number of sub-multiple frequencies from our master 28.63636Mhz crystal oscillator. The following are the primary clocks on the board:

Name	Description
C1	The 3.579545Mhz Color Clock
C2	C1 shifted 45 degrees later
C3	C1 shifted 90 degrees later
C4	C1 shifted 135 degrees later
7M	C1 XORed with C3* (7.15909Mhz)
DAC	7M shifted 90 degrees later

7M is the processor clock for the 68000 microprocessor. C1-C4 and DAC are used to clock the custom chips and for determining the timing of signals to the memory arrays.

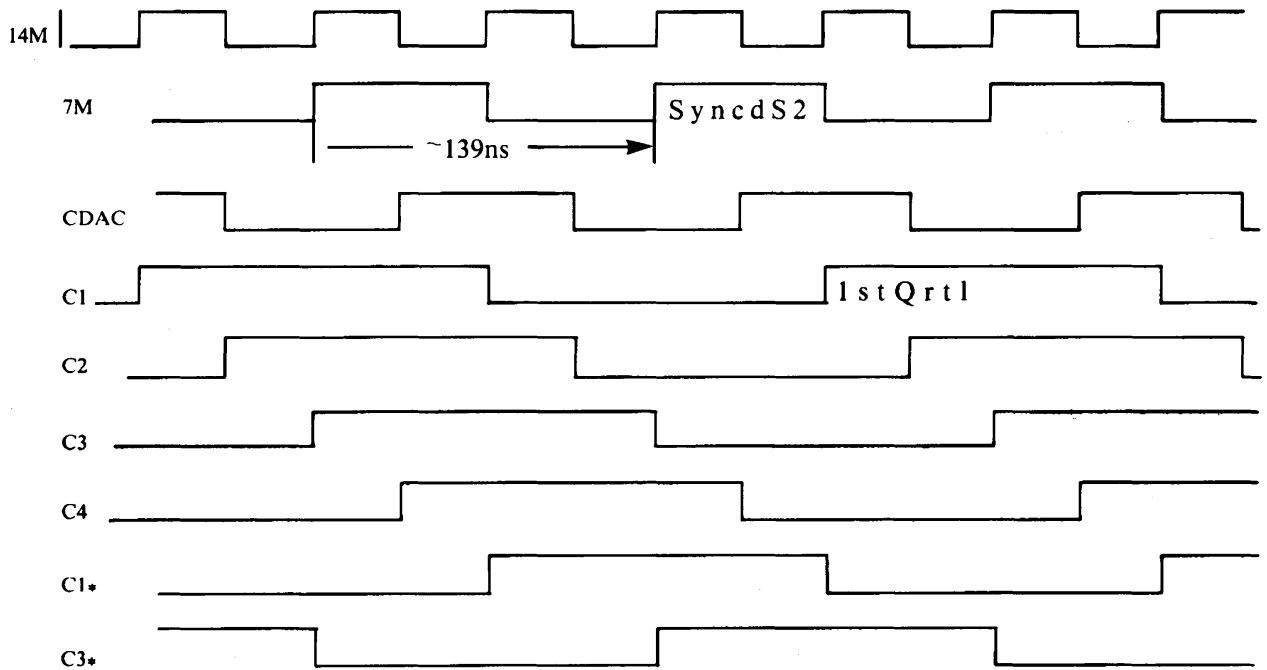
The above frequencies are true for NTSC Amigas. A PAL Amiga will operate slightly slower, with a main clock of 28.37516Mhz. This is divided down to get 7M = 7.09379Mhz and C1 = 3.546895Mhz. A special circuit is required to take five fourths of C1 to derive the PAL colorburst frequency of 4.43361875Mhz.

The following clocks are available at the edge connector:

Name	Pin	Description
C3*	14	C3 inverted
CDAC	15	DAC equivalent
C1*	16	C1 inverted

Note that 7M (the processor clock) is not available at the connector; it can be easily generated by:
 $C3^* \text{ XNOR } C1^* = 7M \text{ equivalent}$

If you need a 14.31818Mhz synchronous clock, you can generate it by:
 $(7M_{equiv}) \text{ XOR } (CDAC) = 14M \text{ equivalent}$



Amiga System Clocks

THEORY OF OPERATION (Continued)**THE 3 CUSTOM CHIPS**

The 3 custom chips provide very fast manipulation of graphics and audio data in the display RAM. All the major functions in the chips are DMA driven; that is, streams of data are moved between the custom chips and display RAM under DMA control. These streams of data are acted upon by the custom chips. Fat Agnus, custom chip #1, contains 25 dedicated purpose DMA counters.

The 3 chips have control registers which are usually loaded by the 68000. However, Fat Agnus also has the capability of loading control registers in the other 2 custom chips. When Fat Agnus performs a bus cycle, it outputs a code on the Register Address Bus telling the other 2 chips the nature of the bus cycle. This is necessary because many of the bus cycles provide data to or from the other 2 chips, thus they must cooperate appropriately.

In addition to manipulating data in the display RAM, the custom chips output streams of data to the **video output** circuits and audio output circuits, and they move data to and from the floppy disks and serial port.

Note that the display RAM buses can be completely isolated from the 68000 buses by Fat Agnus and Data Bus drivers. Thus, Fat Agnus can be performing a bus cycle on the display buses simultaneously with the 68000 performing a bus cycle on its buses. This parallelism increases throughout.

BUS CONTROL, ADDRESS/DATA MUX, ADDRESS DRIVER

The bus control logic resides in the control chip (GARY) and Fat Agnus. They provide 3 major functions, they:

- Synchronize the 68000 to the current phase of C1

- Arbitrate between the 68000 and Fat Agnus for the display buses

- Generate DRAM timing for the video RAM bus drivers appropriate to the current cycle

Synchronizing the 68000 to C1 is straightforward, since the 68000 is clocked by 7M which is twice the frequency and synchronous to C1. If the 68000 starts a bus cycle in the wrong phase of C1, the bus control chip merely delays /DTACK long enough so that the 68000 will complete the bus cycle in the desired phase relationship to C1. This phase relationship is necessary because the custom chips and the display RAM are clocked by C1.

Arbitration is very simple. Fat Agnus tells the bus control prior to taking the display RAM buses by asserting an input to the control chip (GARY) called /DBR. Whenever Fat Agnus has the display buses and the 68000 wants them, the 68000 is held off by not giving it /DTACK. In this state the 68000 has no effect on the display buses until the bus controller enables the bus drivers.

Fat Agnus generates the DRAM timings and does all address multiplexing. If the 68000 is running a video memory cycle, its addresses are routed through Fat Agnus onto the multiplexed address lines. If the custom chips are running a memory cycle the addresses are routed to the multiplexed address lines from internal address register.

DISPLAY RAM

The display RAM is a 512K read/write memory that resides on the RAM address and RAM data buses. It is expandable to 1M bytes by the addition of the RAM expansion module. It is implemented using standard 256K × 1 dynamic RAMs, refreshed by Fat Agnus.

The display RAM is really used for much more than just holding graphics data. It also stores code and data for the 68000.

CUSTOM CONTROL CHIPS

The Amiga's animation, graphics and sound are produced by three custom chips. Fat Agnus (8375), High Res Denise (8373) and Paula (8364). A fourth custom chip, Gary serves as the control chip. The following pages include feature lists, and block diagrams for these chips.

8375 AGNUS 2MEG

GENERAL

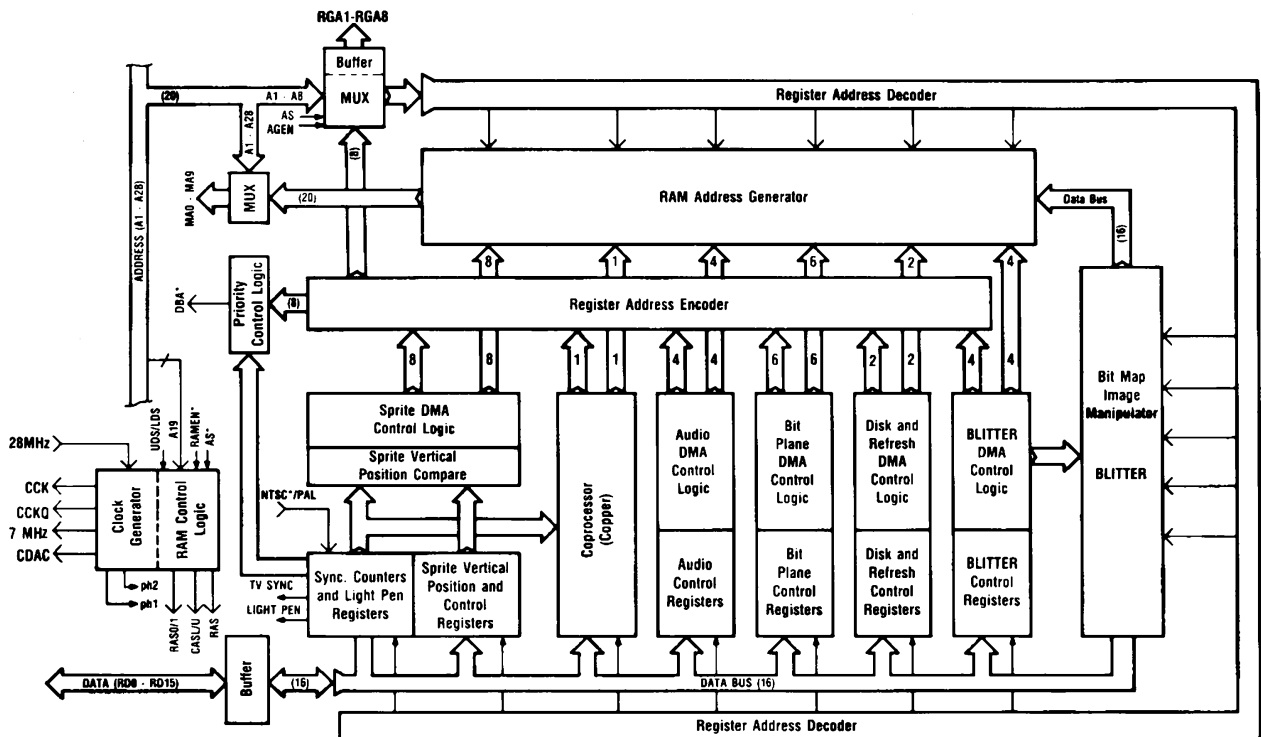
This device is an address generator type IC. Its main function is as a RAM address generator and register address encoder that shall produce all DMA addresses for 25 channels.

The block diagram for this device shows the DMA control and address bus logic. The output of each controller indicates the number of DMA channels driving the Register Address Encoder and RAM Address Generator.

The RAM Address Generator contains an 20 bit pointer register for each of the 25 DMA channels and also it contains pointer restart (backup) registers and jump registers for six (6) of the channels. A full 20 bit adder carries out the pointer increments and adds for jumps.

The priority control logic looks at the pipe-lined DMA request from each controller and stages the DMA cycles based upon their programmed priority and sync counter time slot. Then it signals the processor to get off the bus by asserting the DBR line. The following is a brief description of the device's major operational modes.

A control register determines which 256 possible logic operations is to be performed as the source images are combined and how far they are to be moved (Barrel shifted). In addition to the image combining and movement powers, the Blitter can be programmed to do line drawing or area fill between lines.



Agnus 8375 Block Diagram

BLITTER

The procedure for moving and combining bit mapped images in memory received the name Bit Blit from a computer instruction that did block transfers of data on bit boundaries. These routines became known as Bit Blitters or Blitters. The Blitter DMA Controller is preloaded with the address and size of three (3) source images (A,B, and C) and one (1) destination (D) in the dynamic RAM. These images can be as small as a single character or as large as twice the screen size. They can be full images or smaller windows of a larger image. The actual pixel resolution is controlled by the BLTSIZE (BLTSIZH and BLTSIZV) registers which contain up to 15 bits for the image height (15 bits = 32K dots max.) and up to 11 bits for the image width (11 bits = 2k words = 32K pixels max.). After one word of each source image is sequentially loaded into the source buffer (A, B, C) they are shifted and then combined together in the logic unit to perform image movement overlay, masking, and replacements. The result is captured in the destination buffer (D) and sent back to the RAM memory destination address. This operation is repeated until the complete image has been processed. The unit has extensive pipelining to allow for shifter and logic unit propagation time, while the next set of source words is being fetched.

8375 AGNUS (Continued)

BITPLANE ADDRESSING

Some computer bitmap displays are organized so that the bitplanes for each pixel are all located within the same address. This is called pixel addressing. If the entire data word of one address is used for a single pixel with 8 bit planes, the data word will look like this. (numbers are bitplanes): 12345678-----

The data compression can be improved by packing more than one pixel into a single address like this: 1234567812345678 or like this, if there are only 4 bitplanes: 1234123412341234

The IC device, uses a bitmap technique called Bitplane Addressing. This separates the bitplanes in memory. To create a 4 plane (16 color) image, the bitplane display DMA channels fetch from 4 separate areas of memory like this:

```
1111111111111111
2222222222222222
3333333333333333
4444444444444444
```

These are held in buffer register and are used together as pixels, one bit at a time, by the display (left to right).

This technique allows reduced odd numbers of bitplanes (such as 3 or 5) while maintaining packing efficiency and speed. It also allows grouping bitplanes into 2 separate images, each with independent hardware high speed image manipulation, line draw, and area fill.

DMA CHANNEL FUNCTIONS

Each channel has an 20 bit RAM address pointer that is placed on the MA memory address bus, and is used to select the location of the DMA data transfer from anywhere in 1M words (2M bytes) of RAM.

An eight (8) bit destination address is simultaneously placed on the register address bus (RGA), sending the data to the corresponding register.

In a typical DMA channel, almost all channels have DRAM as source and chip registers as destination.

The pointer must be preloaded and is automatically incremented each time a data transfer occurs.

Each controller utilizes one or more of these DMA channels for its own purposes. The following is a brief summary of these controllers and the DMA channels they use.

A-Blitter (four (4) channels)

The Blitter uses four (4) DMA channels, Three source and one (1) destination as previously described.

Once the Blitter has been started, the four (4) DMA channels are synchronized and pipelined to automatically handle the data transfers without further processor intervention. The images manipulated in memory, independent of the display (bitplane DMA).

B-Bitplane (six (6) channels)

The bitplane controller continuously (during display) transfers display data from memory to display buffer registers. There are six (6) DMA channels to handle the data from six (6) independent bit planes. The buffers convert this bitplane data into pixel data for the display.

C-Copper (one (1) channel)

The Copper is a co-processor that uses one of the DMA channels to fetch its instructions. The DMA pointer is the instruction counter and must be preloaded with the starting address of the Copper's instructions.

The Copper can move (write) data into chip registers. It can skip, jump, and wait (halt). These simple instructions give great power and flexibility because of the following features.

When Copper is halted, it is off the data bus, using no bus cycles until the wait is over. The programmed wait value is compared to a counter that keeps track of the TV beam position (beam counter) and when they are equal, the Copper will resume fetching instructions.

It can cause interrupts, reload the color registers, start the Blitter or service the audio. It can modify almost any register inside or outside the IC device, based on the TV screen coordinates given by the Beam Counter and the actual address encoded on the RGA Bus.

8375 AGNUS (Continued)***DMA CHANNEL FUNCTIONS (Continued)******D-Audio (four (4) channels)***

There are four (4) audio channels, all of which are located outside of the audio DMA Controller section of Agnus. Each controller is independent and uses one DMA channel from the DMA Controller and fetches its data during a dedicated timing slot within horizontal blanking. This is accomplished by a controller asserting the DMAL input on the DMA Controller.

E-Sprites (eight (8) channels)

There are eight (8) independent Sprite controllers, each with its own DMA channel and its own dedicated time slot for DMA data transfer. Sprites are line buffered objects that can move very fast because their positions are controlled hardware registers and comparators.

Each sprite has two (2) sixteen bit data registers that define a 16 pixel wide Sprite with 4 colors. Each has a horizontal position register, a vertical start position register and a vertical stop position register. This allows variable vertical size sprites.

The Sprite DMA controller fetches image and position data automatically from anywhere in 2 Megabytes of memory depending on device pin configuration.

Sprites can be run automatically in DMA mode or they can be loaded and controlled by the microprocessor.

Each Sprite can be re-used vertically as often as desired. Horizontal re-using is also allowed with microprocessor control.

F-Disk (one (1) channel)

The disk controller, which is located outside of the DMA, uses a single DMA channel from the device. The controller uses the DMA time slot for data transfer and can read or write a block of data up to 128K anywhere in 2 Megabytes of memory depending on device pin configuration.

G-Memory Refresh (one (1) channel)

The refresh controller uses a single DMA channel with its own time slots. It places RAS addresses on the memory address bus (MA) during these slots, in order to refresh the dynamic RAM. Memory is refreshed on every raster line.

During the DMA no data transfer actually takes place. The register address bus (RGA) is used to supply video synchronizing codes. At this time RAS1* and RAS are low. CASU* and CASL* are inactive during this cycle.

RAM AND REGISTER ADDRESSING

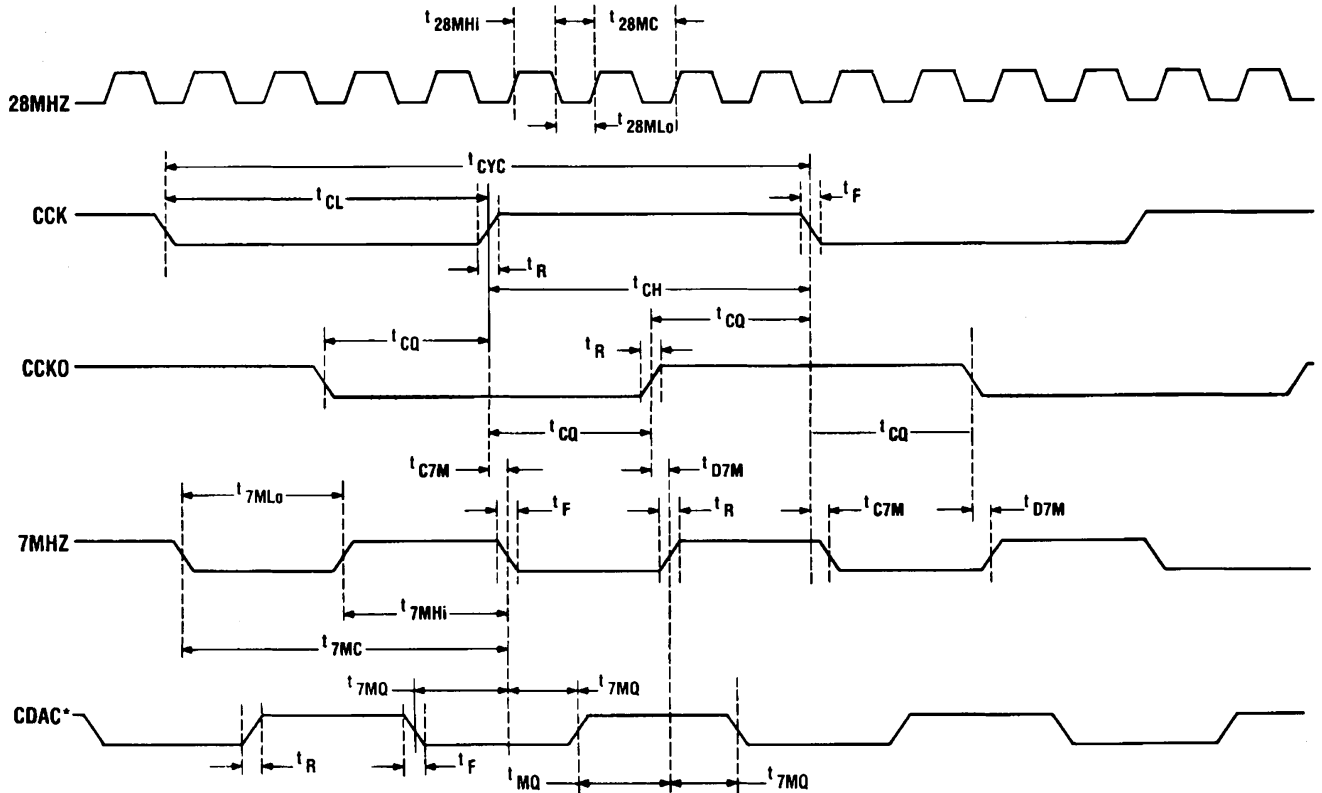
The device generates RAM addresses from two sources, the processor or the device performing DMA cycles. The processor accesses RAM whenever AS* and RAMEN* are both low. At this time, the device also multiplexes the processor address (A1-A20) onto the MA bus. During row address time A9-A17 and A19 are placed onto MA0-MA8, MA9, respectively; during column address time A1-A8, A18 and A20 are placed onto MA0-MA7, MA8 and MA9, respectively. In the 1 meg configuration, A19 is still used to determine the RAS line to be asserted. If A19 is low RAS0* is active and if high RAS1* is active. In the 2 meg option RAS will always be active on a RAM access. The IC will assert CASL* if LDS* is low or CASU* if UDS* is low.

When the device needs to do a DMA cycle, the device disables the processor from accessing RAM by asserting the Data Bus Request Line (DBR*). At this time, the device multiplexes its generated RAM address onto the MA lines and will activate RAS and the proper RAS0* or RAS1* line unless it is a refresh cycle where all RAS lines are active. During a DMA cycle, the IC device will also assert both CASU* and CASL*, unless it is a refresh cycle where they both remain inactive.

The device also generates RGA addresses from either the processor or device DMAs, each of which is selected by an internal multiplexer. This multiplexer allows the processor to perform a register read/write access when AS* and RGEN* are both low. The device then takes the low order byte of the processor address A1 to A8 and reflects its value on the RGA output bus RGA1 to RGA8. The device will reflect the status of PRW input on the RRW output line, to indicate a memory read or write operation.

During a device DMA cycle, the device prevents the processor from doing a register access by asserting the DBR* line. The device will then place the contents of its register address encoder onto the RGA bus.

8375 AGNUS (Continued)



Clock Relations

CLOCK RELATIONS (Refer to Figure above)

	SYMBOL	MIN	MAX	UNIT
2.4.1 28MHz clock cycle	t _{28MC}	34.57		ns
2.4.2 28MHz clock high	t _{28MHi}	12.0		ns
2.4.3 28MHz clock low	t _{28MLo}	12.0		ns
2.4.4 CCK clock cycle	t _{cyC}	260	290	ns
2.4.5 CCK clock high	t _{ch}	130	150	ns
2.4.6 CCK clock low	t _{cl}	130	150	ns
2.4.7 CCK-CCKQ clock separation	t _{cq}	65	75	ns
2.4.8 7MHz clock cycle	t _{7MC}	130	150	ns
2.4.9 7MHz clock high	t _{7MHi}	65	75	ns
2.4.10 7MHz clock low	t _{7MLo}	65	75	ns
2.4.11 7MHz-CDACQ clock separation	t _{7MQ}	30	40	ns
2.4.12 CCK to 7MHz delay	t _{c7M}	0	15	ns
2.4.13 CCKQ to 7MHz delay	t _{q7M}	0	15	ns
2.4.14 Clock rise time	t _r	0	10	ns
2.4.15 Clock fall time	t _f	0	10	ns

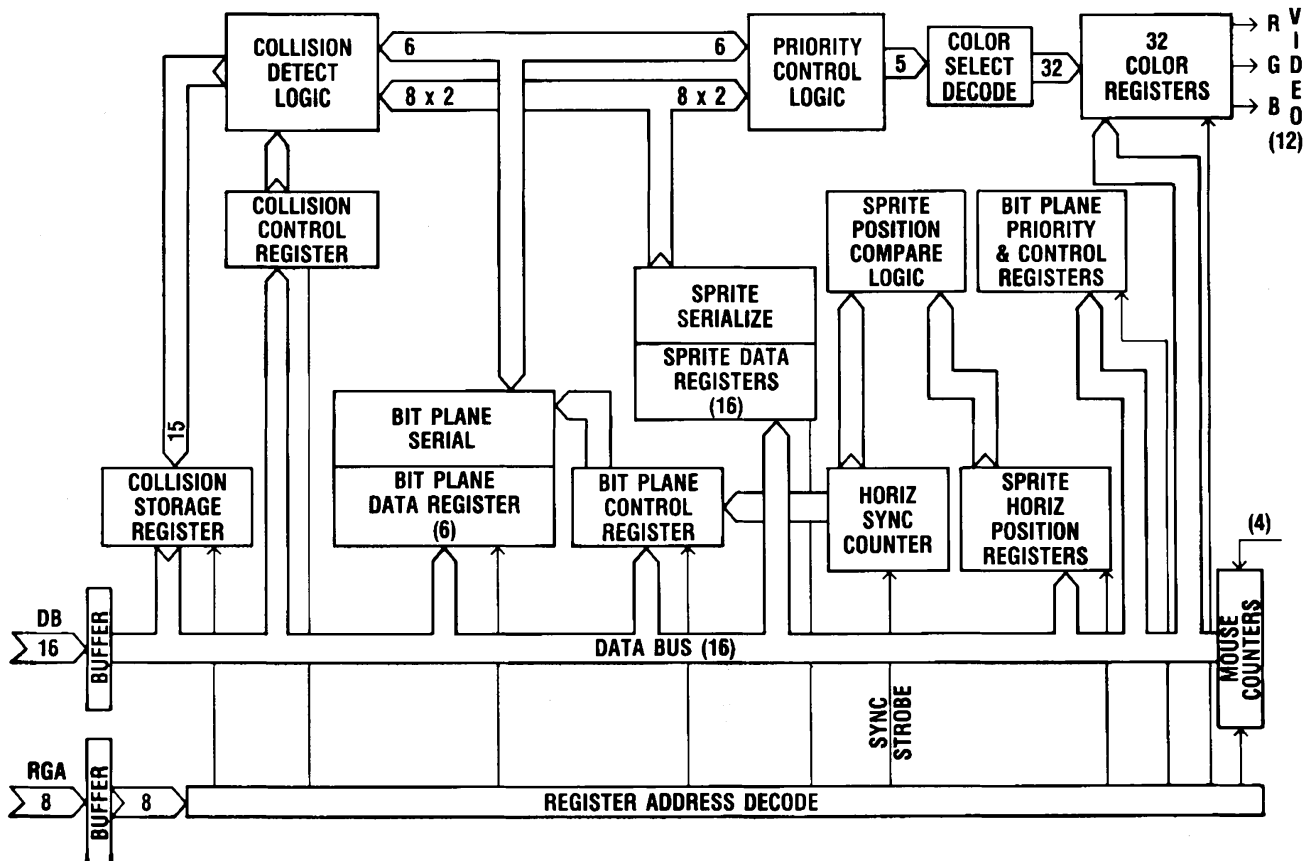
8373 DENISE HI RES

MAIN FUNCTIONS

- Display data buffer, encode display object to RGB colors.
- Bitplane & Sprite display. Parallel data from data bus is retained in six (6) Bitplane and eight pairs of Sprite data buffers.
- Bitplane Data loaded and serialized during display activity.
- Sprite Data loaded during display inactivity — individual serialization occurs when Sprite position Compare logic detects equality between the Sync Counter and any Sprite Position Register.
- Six (6) lines of Bitplane & eight (8) pairs of serial data go to Priority control logic which selects only one (1) of the Sprites or one (1) of the separate Bitmap images to produce the five (5) bit color select code at its output. This five (5) bit code then selects one of the thirty-two (32) color registers to produce the twelve (12) bit RGB video output.
- The Bitplane and Sprite serial lines also go to the Collision Detect Logic, which detects real time coincidence between them, and sets appropriate bits in the Collision Storage register. This register is read and cleared by the 68000.
- The four (4) “mouse counters” are controlled by the two (2) mouse-joystick connectors. These count the pulses representing the horizontal and vertical motion of two (2) “mouse” controllers, and are read by the 68000.

CHIP ELEMENTS

32 Color Registers; Bitplane Priority and Control Registers; Color Select Decoder; Priority Control Logic; 16 Sprite Serial Lines; Sprite Data Registers; Bit Plane Control Registers; Two (2) Mouse Connectors; Sprite Position Compare Logic; Sprite Horizontal Control Registers; Bit Plane Serializer Collision Detect Logic; Collision Control Register; Collision Storage Register; Buffer — Data Bus; Buffer — Register Address Decode; Bit Plane Data Registers Video: RGB; Sprite Serialization.



Denise Block Diagram

8364 PAULA

Paula is the Port, Audio and Uart chip. Its main function is the four audio channels. It also contains the I/O ports, (Disk and Pots), Serial Port (Uart), and the Interrupt Control and Status Register.

D TO A CONVERTERS

The four audio channels each have a DMA pointer register, data register, period, (frequency), register and volume register. Each channel has an on chip D to A (digital to analog) converter on the output. The four channels are grouped into a right and left audio output.

DISK CONTROL

The disk controller has registers for data read, data write and control. It also contains a Precompensation Output circuit, a Data separator input circuit with a digital phase lock loop.

UART CONTROL

The serial port uart included in Paula contains Data registers, Control registers, Transmit, (TRN), and receive registers.

POT CONTROL

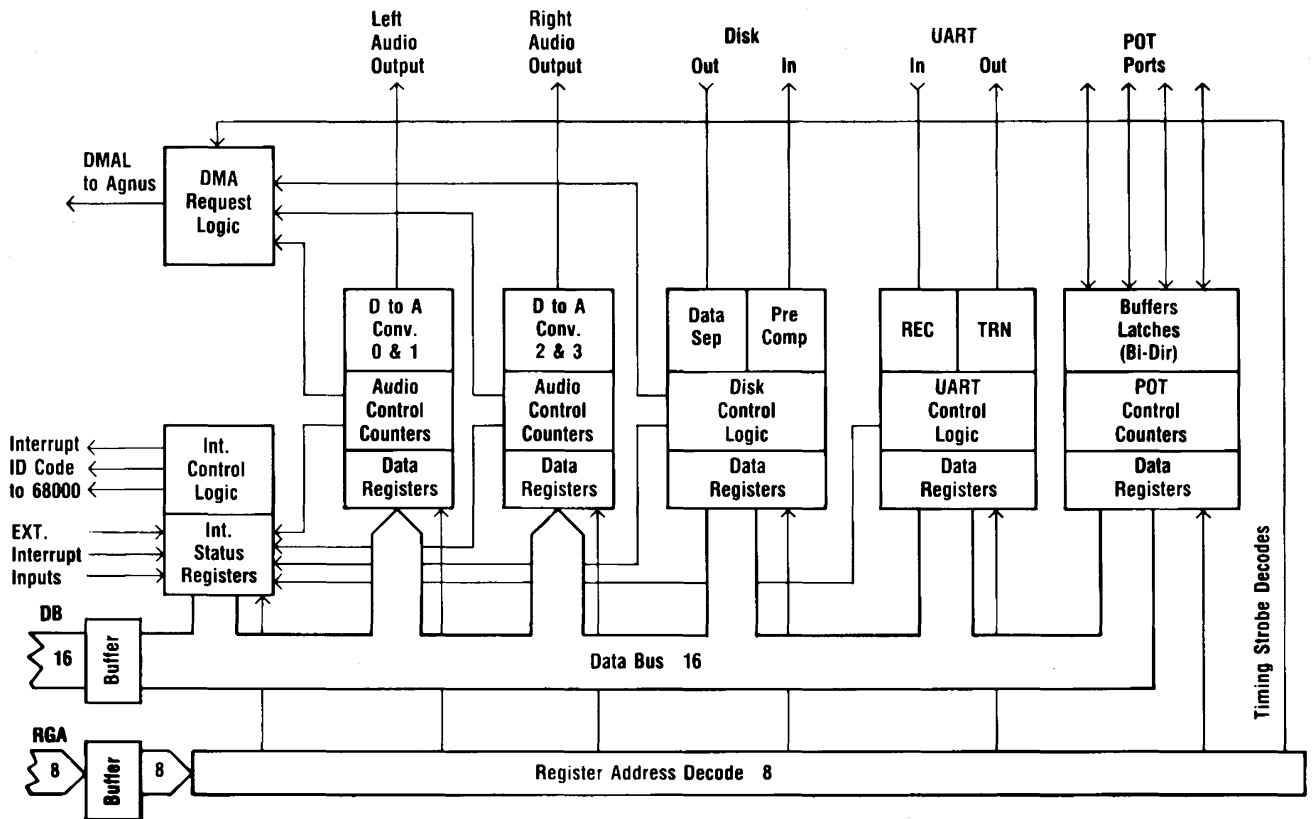
The four pot ports are general purpose I/O ports. They have counters for simple A to D (digital to analog) conversion of an external capacitor charging, which could also be used for analog joystick controllers.

INTERRUPT CONTROL

The audio, disk and uart controllers all set their own Interrupt Status register bits.

DMA REQUEST LOGIC

The audio and disk controllers also go to the DMA request logic, (remember: they are DMA users), causing the DMAL signal to request DMA cycles from Agnus.



Paula Block Diagram

GARY CUSTOM CONTROL CHIP

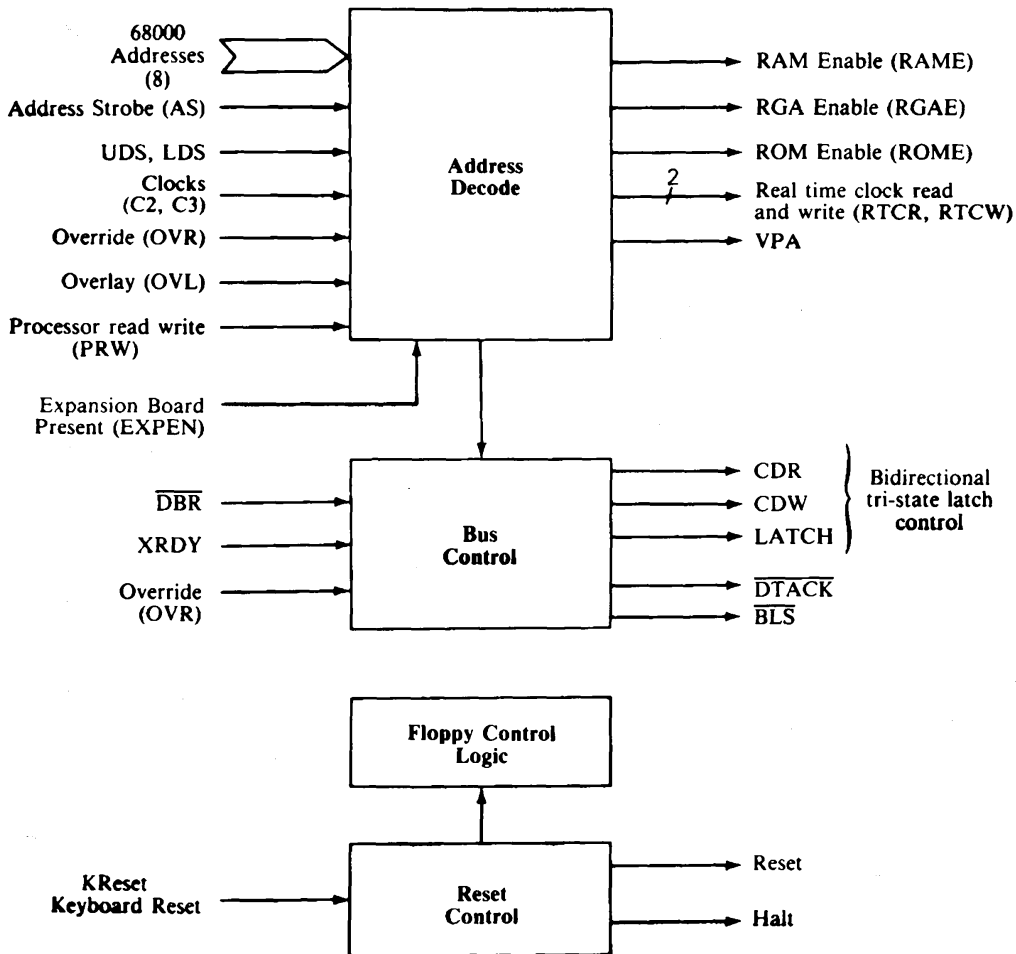
FEATURES

- Provides all bus control signals.
- Provides all address decoding.
- Generates the 68000 VPA signal.
- Handles some of the floppy circuitry.
- Provides keyboard reset interface.

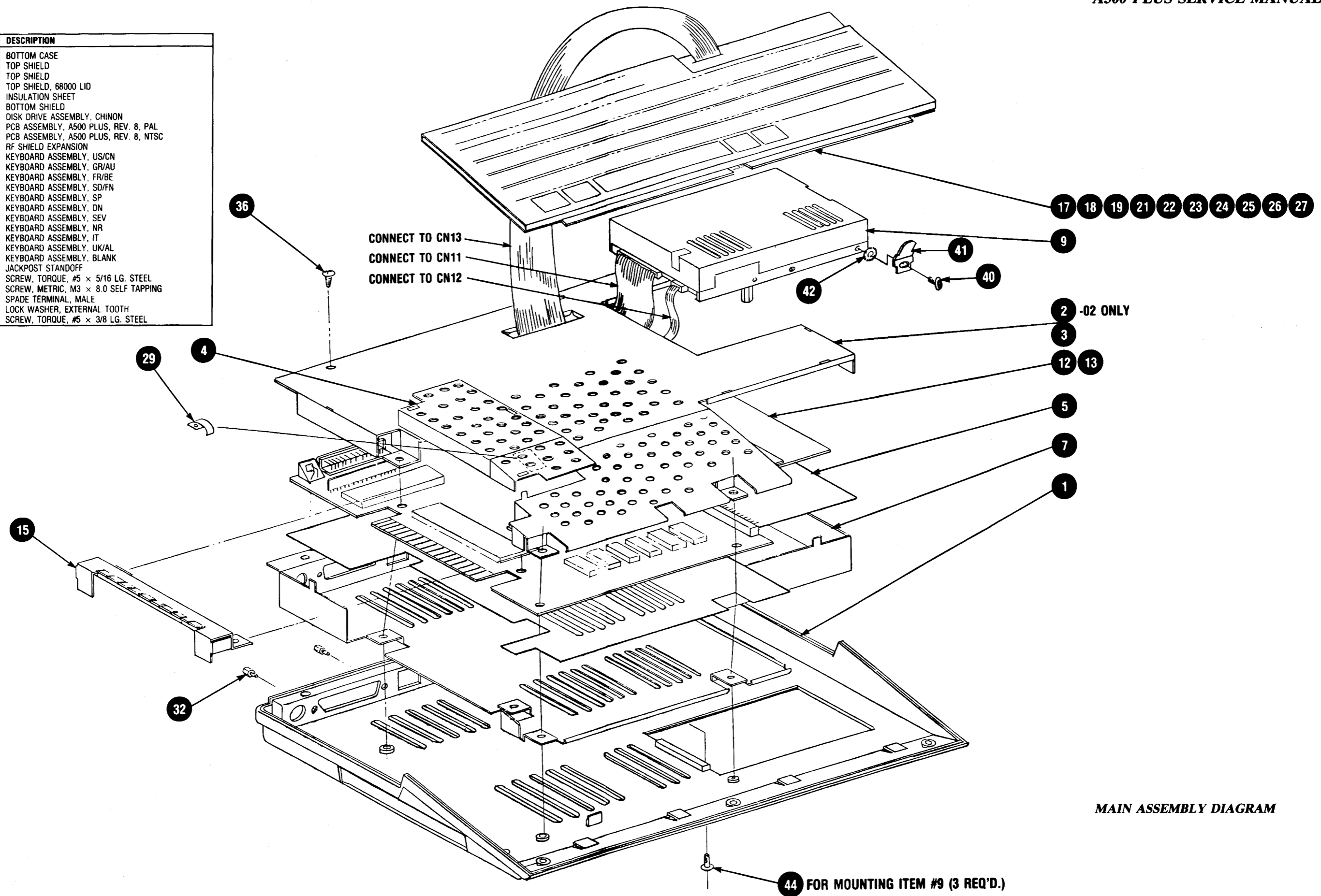
For signal descriptions,
see Schematic #312813, sheet 1 of 10

GND1	1	48	Vcc3
VPA	2	47	MTRX
DEL	3	46	MTRON
DEB	4	45	DKWDB
KBRESET	5	44	DKWEB
Vcc1	6	43	DTACK
MTR	7	42	HLT
DKWE	8	41	RST
DKWD	9	40	GND3
LDS	10	39	A23
UDS	11	38	A22
R/W	12	37	A21
AS	13	36	A20
BGACK	14	35	A19
BLIT	15	34	A18
SEL	16	33	A17
Vcc2	17	32	EXRAM
REGEN	18	31	XRDY
BLISS	19	30	OVL
RAMEN	20	29	OVR
ROMEN	21	28	CCK
CLKRD	22	27	CCKQ
CLKWR	23	26	CDAC
GND2	24	25	LATCH

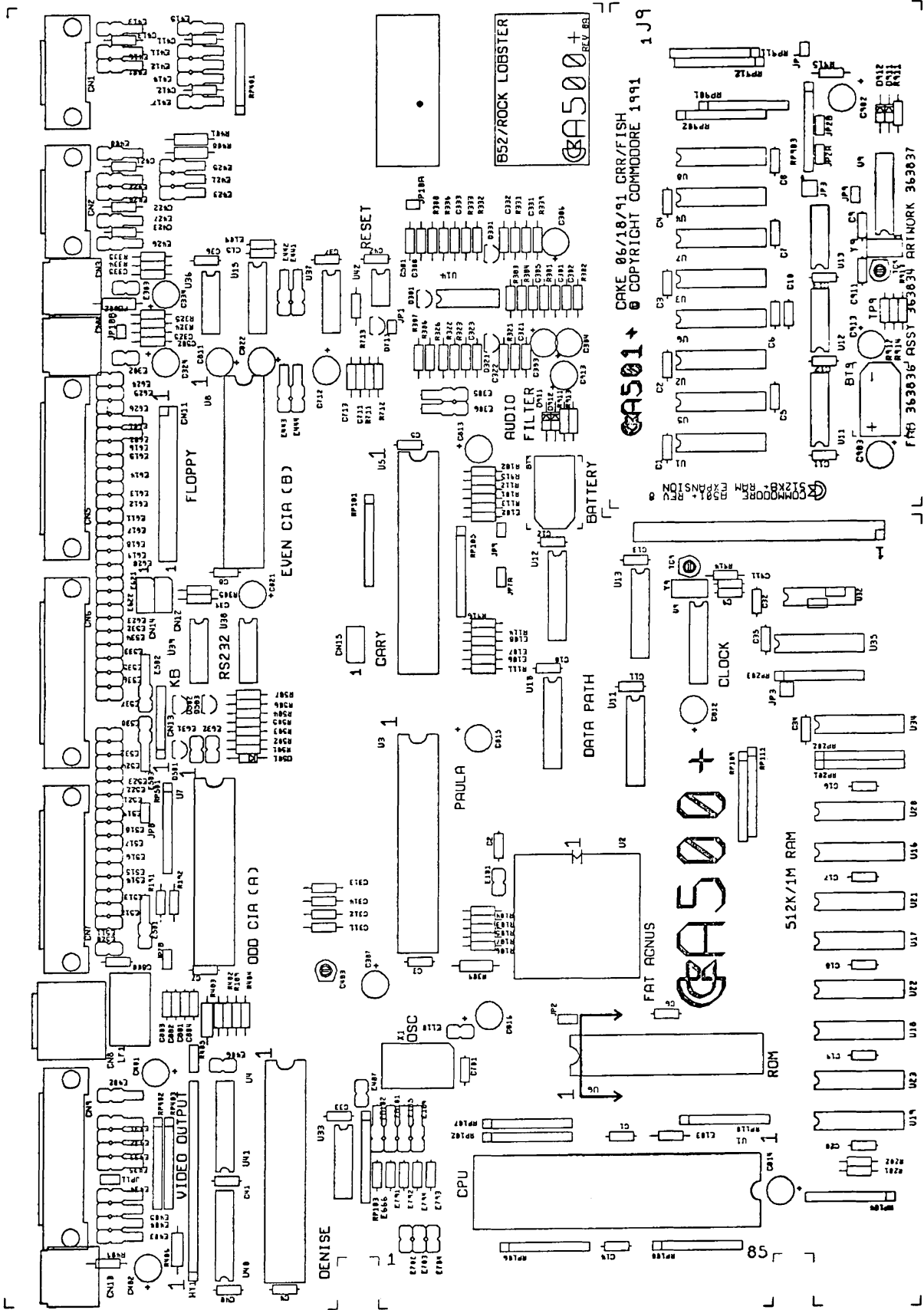
GARY BLOCK DIAGRAM



ITEM NO.	PART NO.	DESCRIPTION
1	312506-01	BOTTOM CASE
2	332358-01	TOP SHIELD
3	312504-02	TOP SHIELD
4	332359-01	TOP SHIELD, 68000 LID
5	312589-01	INSULATION SHEET
7	312590-01	BOTTOM SHIELD
9	312594-01	DISK DRIVE ASSEMBLY, CHINON
12	312812-01	PCB ASSEMBLY, A500 PLUS, REV. 8, PAL
13	312812-02	PCB ASSEMBLY, A500 PLUS, REV. 8, NTSC
15	327038-01	RF SHIELD EXPANSION
17	312502-01	KEYBOARD ASSEMBLY, US/CN
18	312502-02	KEYBOARD ASSEMBLY, GR/AU
19	312502-03	KEYBOARD ASSEMBLY, FR/BE
20	312502-05	KEYBOARD ASSEMBLY, SD/FN
21	312502-06	KEYBOARD ASSEMBLY, SP
22	312502-07	KEYBOARD ASSEMBLY, DN
23	312502-08	KEYBOARD ASSEMBLY, SEV
24	312502-09	KEYBOARD ASSEMBLY, NR
25	312502-04	KEYBOARD ASSEMBLY, IT
26	312502-12	KEYBOARD ASSEMBLY, UK/AL
27	312504-99	KEYBOARD ASSEMBLY, BLANK
32	390251-01	JACKPOST STANDOFF
36	390146-01	SCREW, TORQUE, #5 x 5/16 LG. STEEL
40	906800-03	SCREW, METRIC, M3 x 8.0 SELF TAPPING
41	252177-01	SPADE TERMINAL, MALE
42	905650-11	LOCK WASHER, EXTERNAL TOOTH
44	390146-02	SCREW, TORQUE, #5 x 3/8 LG. STEEL



MAIN ASSEMBLY DIAGRAM



A500 PLUS PCB ASSEMBLY 312812

Commodore International Spare Parts List

A500 PLUS SHIPPING ASSEMBLIES

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SHIPPING ASSY A500 PLUS	SHIPPING ASSY A500 PLUS (Continued)		
535008-01	U.S.	315938-01	SOFTWARE SUB ASSY U.S.
535008-02	CN	315938-02	SOFTWARE SUB ASSY CN
535008-03	UK	315938-03	SOFTWARE SUB ASSY UK
535008-04	GR	315938-04	SOFTWARE SUB ASSY GR
535008-05	FR	315938-05	SOFTWARE SUB ASSY FR
535008-06	IT	315938-06	SOFTWARE SUB ASSY IT
535008-07	SP	315938-07	SOFTWARE SUB ASSY SP
535008-08	SG	315938-08	SOFTWARE SUB ASSY SG
535008-09	SF	315938-09	SOFTWARE SUB ASSY SF
535008-10	AU (NOT USED)	315938-10	SOFTWARE SUB ASSY NR
535008-11	NR	315938-11	SOFTWARE SUB ASSY SD
535008-12	SD	315938-12	SOFTWARE SUB ASSY FN
535008-13	FN	315938-13	SOFTWARE SUB ASSY NE
535008-14	NE	315938-14	SOFTWARE SUB ASSY DN
535008-15	DN	315938-15	SOFTWARE SUB ASSY BF
535008-16	BF	315938-16	SOFTWARE SUB ASSY AL
535008-17	BD (NOT USED)	315938-17	SOFTWARE SUB ASSY PG
535008-18	AL	318994-01	QUICK CONNECT FOR A500
535008-19	CEL (NOT USED)	363328-01	INTRODUCING THE A500 ENGLISH
535008-20	PG	368382-01	INTRODUCING THE A500 GERMAN
319999-02	BOX MASTER SHIPPING A500 PLUS (SUB FOR 319999-03)	368383-01	INTRODUCING THE A500 FR
312585-03	BOX PACKING A500 PLUS	368384-01	INTRODUCING THE A500 IT
363642-01	MAIN ASSY US/CN	368385-01	INTRODUCING THE A500 SP
363642-02	MAIN ASSY GR/AU	368388-01	INTRODUCING THE A500 NR
363642-03	MAIN ASSY FR/BE	368389-01	INTRODUCING THE A500 SW
363642-04	MAIN ASSY SD/FN	368390-01	INTRODUCING THE A500 FINNISH
363642-05	MAIN ASSY SP	368391-01	INTRODUCING THE A500 DUTCH
363642-06	MAIN ASSY DN	368392-01	INTRODUCING THE A500 DANISH
363642-07	MAIN ASSY SEV	368395-01	INTRODUCING THE A500 PORTUGUESE
363642-08	MAIN ASSY NR	368398-01	QUICK CONNECT GUIDE A500 GERMAN
363642-09	MAIN ASSY NE/AL	368399-01	QUICK CONNECT GUIDE A500 FR
363642-10	MAIN ASSY UK	368400-01	QUICK CONNECT GUIDE A500 ITALIAN
363642-11	MAIN ASSY IT	368401-01	QUICK CONNECT GUIDE A500 SPANISH
363642-12	MAIN ASSY PG	368404-01	QUICK CONNECT GUIDE A500 NORWEGIAN
363642-99	MAIN ASSY BLANK KEYBOARD	368405-01	QUICK CONNECT GUIDE A500 SWEDISH
251006-03	POLYBAG ANTI STATIC	368406-01	QUICK CONNECT GUIDE A500 FINNISH
324257-01	BAG DRYING AGENT	368407-01	QUICK CONNECT GUIDE A500 DUTCH
312583-01	ENDCAP LEFT	368408-01	QUICK CONNECT GUIDE A500 DANISH
312583-02	ENDCAP RIGHT	368411-01	QUICK CONNECT GUIDE A500 PORTUGUESE
380928-01	MILL BOARD WITH FOAM		
312503-01	POWER SUPPLY UL/CSA 110V		
312503-02	POWER SUPPLY BSI 240V		
312503-03	POWER SUPPLY VDE 220V		
312503-04	POWER SUPPLY SEV 220V		
312503-05	POWER SUPPLY SAA 220V		
327124-02	MOUSE ASSY		
390925-01	CABEL 25 PIN SCART TO 23 PIN D SUB W/2 R FOR TV CONN		
318143-02	GLUE WHITE		
380929-01	MILLBOARD		
368084-01	SEAL TAMPER EVIDENT (PLACE ON BOX FLAPS)		
311847-01	PLASTIC HANDLE		
999104-01	ADHESIVE TAPE TRANSPARENT 50MM (ON MASTER SHIP BOX FLAPS)		
310397-01	BOX ACCESSORY		
332417-01	SPACER CARDBOARD		
332263-01	SHEET TOP/BOTTOM		
332264-01	SHEET SIDE		
390533-01	POWER PLUG FUSED U.K.		

Commodore International Spare Parts List

A500 PLUS MAJOR ASSEMBLIES

Commodore part numbers are provided for reference only and do not indicate the availability of spare parts from Commodore. Industry standard parts (Resistors, Capacitors, Connectors) should be secured locally. Part number information may vary according to country, some parts may not be available in all countries.

MAIN ASSY A500 PLUS		AMIGA CONSUMER SOFTWARE SUB ASSEMBLY V2.0	
363642-01	MAIN ASSY A500 PLUS U.S./CANADA	315938-01	AMIGA CONSUMER SOFTWARE SUB ASSEMBLY U.S.A.
363642-02	MAIN ASSY A500 PLUS GERMANY/AUSTRIA	315938-02	AMIGA CONSUMER SOFTWARE SUB ASSEMBLY CANADA
363642-03	MAIN ASSY A500 PLUS FRANCE/BELGIUM	315938-03	AMIGA CONSUMER SOFTWARE SUB ASSEMBLY U.K.
363642-04	MAIN ASSY A500 PLUS SWEDEN/FINLAND	315938-04	AMIGA CONSUMER SOFTWARE SUB ASSEMBLY GERMANY
363642-05	MAIN ASSY A500 PLUS SPAIN/S. AMERICA	315938-05	AMIGA CONSUMER SOFTWARE SUB ASSEMBLY FRANCE
363642-06	MAIN ASSY A500 PLUS DENMARK	315938-06	AMIGA CONSUMER SOFTWARE SUB ASSEMBLY ITALY
363642-07	MAIN ASSY A500 PLUS SWITZERLAND	315938-07	AMIGA CONSUMER SOFTWARE SUB ASSEMBLY SPAIN
363642-08	MAIN ASSY A500 PLUS NORWAY	315938-08	AMIGA CONSUMER SOFTWARE SUB ASSEMBLY SWITZERLAND-GERMAN
363642-09	MAIN ASSY A500 PLUS NETHERLANDS	315938-09	AMIGA CONSUMER SOFTWARE SUB ASSEMBLY SWITZERLAND-FRENCH
363642-10	MAIN ASSY A500 PLUS U.K.	315938-10	AMIGA CONSUMER SOFTWARE SUB ASSEMBLY NORWAY
363642-11	MAIN ASSY A500 PLUS ITALY	315938-11	AMIGA CONSUMER SOFTWARE SUB ASSEMBLY SWEDEN
363642-12	MAIN ASSY A500 PLUS PORTUGAL	315938-12	AMIGA CONSUMER SOFTWARE SUB ASSEMBLY FINLAND
363642-99	MAIN ASSY A500 PLUS BLANK KEYBOARD PAL	315938-13	AMIGA CONSUMER SOFTWARE SUB ASSEMBLY NETHERLANDS
312506-01	BOTTOM CASE	315938-14	AMIGA CONSUMER SOFTWARE SUB ASSEMBLY DENMARK
332358-01	TOP SHIELD	315938-15	AMIGA CONSUMER SOFTWARE SUB ASSEMBLY BELGIUM-FRENCH
312504-02	TOP SHIELD (SUB FOR 332358-01 & 332359-01)	315938-16	AMIGA CONSUMER SOFTWARE SUB ASSEMBLY AUSTRALIA
332359-01	TOP SHIELD 68000 LID (USE W/332358-01)	315938-17	AMIGA CONSUMER SOFTWARE SUB ASSEMBLY PORTUGAL
312589-01	INSULATION SHEET	368244-01	MANUAL USING THE AMIGA WORKBENCH ENGLISH
312590-01	BOTTOM SHIELD	367813-01	DISK ASSY WORKBENCH 2.04 U.S. (INTERNATIONAL) 3.5"
312594-01	DISK DRIVE ASSY CHINON	367814-01	DISK ASSY WORKBENCH 2.04 CANADIAN-FRENCH 3.5"
312594-02	DISK DRIVE ASSY PANASONIC (SUB FOR 312594-01)	367815-01	DISK ASSY WORKBENCH 2.04 U.K. 3.5"
312812-01	PCB ASSY A500 PLUS REV 8 PAL	367816-01	DISK ASSY WORKBENCH 2.04 GERMAN 3.5"
312812-02	PCB ASSY A500 PLUS REV 8 NTSC	367817-01	DISK ASSY WORKBENCH 2.04 FRENCH/BELGIUM 3.5"
327038-01	RF SHIELD EXPANSION	367818-01	DISK ASSY WORKBENCH 2.04 ITALIAN 3.5"
312502-01	KEYBOARD ASSY U.S./CAN	367819-01	DISK ASSY WORKBENCH 2.04 SPANISH 3.5"
312502-02	KEYBOARD ASSY GR/AU	367820-01	DISK ASSY WORKBENCH 2.04 SWISS 3.5"
312502-03	KEYBOARD ASSY FR/BE	367821-01	DISK ASSY WORKBENCH 2.04 NORWEGIAN 3.5"
312502-04	KEYBOARD ASSY IT	367822-01	DISK ASSY WORKBENCH 2.04 SWEDISH/FINNISH 3.5"
312502-05	KEYBOARD ASSY SD/FN	367823-01	DISK ASSY WORKBENCH 2.04 DANISH 3.5"
312502-06	KEYBOARD ASSY SP	367824-01	DISK ASSY EXTRAS 2.04 INTERNATIONAL 3.5"
312502-07	KEYBOARD ASSY DN	367825-01	DISK ASSY FONTS 2.04 INTERNATIONAL 3.5"
312502-08	KEYBOARD ASSY SEV	318843-01	DISKETTE FOLDER 3.5"
312502-09	KEYBOARD ASSY NR	318896-04	SOFTWARE LICENSE AGREEMENT ENGLISH
312502-12	KEYBOARD ASSY UK	318708-02	SOFTWARE LICENSE AGREEMENT GERMAN
312502-99	KEYBOARD ASSY BLANK	380913-02	POLY BAG CATCH 120MM X 170MM
312472-01	KEYBOARD SUPPORT	400808-01	SERVICE SUB ASSY A500 SERIES
390251-01	JACKPOST STANDOFF	318882-01	CARD WARRANTY CANADA
390251-03	JACKPOST STANDOFF (SUB FOR 390251-01)	325249-01	CARD WARRANTY U.K.
324530-02	JACKPOST STANDOFF (SUB FOR 390251-01)	320046-06	CARD WARRANTY GERMANY
390146-01	SCREW TORQUE #5 X 5/16 LG STEEL (QTY 4) USE ON TOP SHIELD & RF	325254-01	CARD WARRANTY FRANCE
390177-01	SCREW TORQUE #5 X 5/16 LG (SUB FOR 390146-01)	332408-01	CARD WARRANTY SWITZERLAND
906883-03	SCREW PAN HEAD 2.9 X 8 SELF TAPPING (SUB FOR 390146-01)	368014-01	CARD WARRANTY AUSTRALIA
906800-03	SCREW METRIC M3 X 8.0 SELF TAPPING (QTY 4 — USE W/312594-01)	312341-02	CARD DISK REPLACEMENT U.S.
252177-01	SPADE TERMINAL MALE	318556-02	CARD DISK REPLACEMENT CANADA
905650-11	LOCK WASHER EXTERNAL TOOTH	368363-01	MANUAL USING THE AMIGA WORKBENCH FRENCH
390146-02	SCREW TORQUE #5 X 3/8 LG STEEL (QTY 6 — USE W/312506-01)	368364-01	MANUAL USING THE AMIGA WORKBENCH ITALIAN
390177-02	SCREW TORQUE #5 X 3/8 LG (SUB FOR 390146-02)	368365-01	MANUAL USING THE AMIGA WORKBENCH GERMAN
906883-04	SCREW PAN HEAD 2.9 X 9.5 SELF TAPPING (SUB FOR 390146-02)	368366-01	MANUAL USING THE AMIGA WORKBENCH SPANISH
312591-01	RAM EXPANSION DOOR	368367-01	MANUAL USING THE AMIGA WORKBENCH DANISH
312595-01	COVER EXPANSION	368368-01	MANUAL USING THE AMIGA WORKBENCH DUTCH
312505-02	TOP CASE	368369-01	MANUAL USING THE AMIGA WORKBENCH NORWEGIAN
363946-02	NAMEPLATE	368370-01	MANUAL USING THE AMIGA WORKBENCH SWEDISH
950150-03	RUBBER FEET		
363641-01	LABEL RATING PAL (MADE IN GERMANY)		
363641-02	LABEL RATING NTSC (MADE IN GERMANY)		
363641-03	LABEL RATING PAL (MADE IN USA) (SUB FOR 363641-01)		
363641-04	LABEL RATING NTSC (MADE IN USA) (SUB FOR 363641-02)		
363641-05	LABEL RATING PAL (MADE IN HONG KONG)		
363641-06	LABEL RATING NTSC (MADE IN HONG KONG)		
363641-07	LABEL RATING PAL (MADE IN PHILIPPINES)		
363641-08	LABEL RATING NTSC (MADE IN PHILIPPINES)		
316416-01	LABEL WARNING POWER OFF		
325090-02	STICKER SEAL WARRANTY		
364137-01	SPRING FINGER		
363641-09	LABEL RATING PAL (MADE IN HK)		
363641-10	LABEL RATING NTSC (MADE IN HK)		
332348-01	TAPE MYLAR		
366648-01	LABEL BAR CODE BLANK		
366649-01	LABEL BAR CODE BLANK		

Commodore International Spare Parts List

A500 PLUS PCB Components

PCB Assembly #312812 (-01 — PAL; -02 — NTSC)

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IC COMPONENTS			CAPACITORS (Continued)		
901882-01	MC1488	U38	900463-16	MLC AXIAL X7R 1000 PF	C411-C413, C421-C423
901883-01	MC1489	U39	900463-23	MLC AXIAL X7R 3900 PF	C323, C333
390086-01	LF347	U14	900463-26	MLC AXIAL X7R 6800 PF	C322, C332
901523-01	NE555	U42	900463-36	MLC AXIAL X7R .047 UF	C311-C314
390084-03	MC68000 8 MHZ	U1	900463-37	MLC AXIAL X7R .1 UF	C321, C331
318072-01	MOS 5719 R2 GARY	U5	251894-18	ELEC ALUM RAD 1000 UF 10V	C307, C401, C402
390979-01	ROM 256K X 16 KICKSTART 2.04	U6	251894-50	ELEC ALUM RAD 47 UF 35V	C821, C822
252127-02	MOS 8364 R7 PAULA	U3	390101-02	ELEC ALUM RAD 100 UF 16V	C811-C816
390544-01	MOS 8375 AGNUS 2 MEG PAL	U2	390101-04	ELEC ALUM RAD 22 UF 35V	C303, C304, C324, C334
390544-02	MOS 8375 AGNUS 2 MEG NTSC	U2	390101-06	ELEC ALUM RAD 10 UF 35V	C306, C712
318029-02	MOS 8520 R4 AMIGA CIA	U7, U8	900410-13	ELEC TANT RAD 4.7 UF 16V	C913
318050-01	74F244	U35	RESISTORS — 1/4W, 5%		
318052-01	74F258	U33	901550-01	CF 1K	R191, R192, R303-R305, R324, R334, R713, R915, R916
318073-01	OKI MSM6242B RTC	U9	901550-19	CR 4.7K	R201, R202, R402, R403, R404, R503, R504
318099-04	DRAM 256K X 4 120NS	U16-U23	901550-20	CF 10K	R306, R308, R322, R323, R332, R333, R339, R501, R505, R506, R914
318099-02	DRAM 256K X 4 100NS (SUB FOR -04)	U16-U23	901550-22	CF 47K	R712
390227-06	74HCT245	U40, U41	901550-23	CF 2.7K	R307, R502
390090-01	74FF139	U32	901550-49	CF 100 OHM	R507
390108-01	74F373	U34	901550-56	CF 47 OHM	R103-R107, R113
390229-03	VIDEO HYBRID	HY1	901550-57	CF 390 OHM	R325, 335
390433-02	MOS 8373 R4 DENISE HI RES	U4	901550-58	CF 470 OHM	R911, R913
901521-11	74LS157	U15	901550-64	CF 10 OHM	R301, R302
901521-13	74LS244	U10, U12	901550-82	CF 470K	R326, R336
901521-29	73LS373	U11, U13	901550-84	CF 1 MEG OHM	R711
901521-31	73LS32	U37	901550-89	CF 150 OHM	R409, FB102
901521-37	74LS05	U36	901550-90	CF 27 OHM	R101, R102
390433-01	MOS 8373 R3 DENISE HI RES	U4	901550-94	CF 68 OHM	R109, R111, R112, R114, E104, E105, FB101
IC SOCKETS			901550-108	CF 360 OHM	R321, R331
904150-06	40 PIN DIP	U7, U8	RESISTORS — 1/2W, 5%		
904150-10	64 PIN DIP	U1	901600-55	CF 0.47 OHM	R405
390185-01	84 PIN PLCC	U2	901600-15	CF 47 OHM	E501-E503
251313-01	48 PIN DIP	U3-U5	901600-36	CF 1 OHM	R309
251313-02	48 PIN DIP (SUB FOR -01)	U3-U5	901600-50	CF 4.7 OHM	R401, R406, R408
904150-09	42 PIN DIP	U6	901600-48	CF 5.1 OHM (SUB FOR -50)	R401, R406, R408
CONNECTORS			RESISTOR NETWORKS		
252122-01	RCA JACK WHITE AUDIO	CN4	390227-05	68 OHM SIP 10 PIN 5 ELE	RP201-RP203
252122-03	RCA JACK YELLOW COMPOSITE	CN10	390227-06	47 OHM SIP 10 PIN 5 ELE	RP402, RP403
252122-04	RCA JACK BLACK AUDIO	CN3	390227-08	39 OHM SIP 10 PIN 5 ELE	RP103
390248-01	RCA JACK METAL (SUB FOR 252122-01 & -04)	CN3, CN4, CN10	390227-03	22 OHM SIP 10 PIN 5 ELE (SUB FOR -08)	RP103
252167-01	5 PIN SQUARE DIN POWER	CN8	902410-07	10K SIP 10 PIN 9 ELEMENT	RP501
325516-04	4 PIN FLOPPY POWER (INT. FLOPPY PWR.)	CN12	902410-08	4.7K SIP 10 PIN ELEMENT	RP101, RP102, RP401
903345-17	HEADER 34 PIN W/KEY (INTERNAL FLOPPY)	CN11	902410-11	470 OHM SIP 10 PIN 9 ELEMENT	RP104
350903-01	HEADER 34 PIN W/KEY (SUB FOR 903345-17)	CN11	MISCELLANEOUS		
390224-01	HEADER 56 PIN MALE RT ANGLE (EXPANSION)	P9	380393-01	BATTERY NICAD 3.6V 60MAH	BT9
390241-03	D SUB 23 PIN FEMALE DB23s EXT. FLOPPY	CN5	251842-02	EMI FILTER 100 PF	E511-E519, E521-E524, E611-E626, E631, E632
390241-05	D SUB 25 PIN FEMALE CB25s (CENTRONICS)	CN7	390275-01	EMI FILTER 6800 PF	E302, E303, E411-E414, E421-E424
390242-01	D SUB 9 PIN MALE DB9p (JOYSTICK)	CN1, CN2	390275-02	EMI FILTER 150 PF	E402, E434, E532, E534
390242-03	D SUB 23 PIN MALE DB23p (VIDEO)	CN9	390297-01	EMI FILTER 270 PF	E305, E306
390242-05	D SUB 25 PIN MALE DB25p (RS-232)	CN6	390297-04	EMI FILTER 470 PF	E415-E417, E425-E427, E441-E444, E520, E531, E533, E535-E538
903326-08	8 PIN SIL W/KEY (KEYBOARD)	CN13	390297-05	EMI FILTER .01 UF	E101, E110, E401, E403-E408, E601, E602, E702-E704
OSCILLATORS, TRANSISTORS AND DIODES			251578-02	LINE FILTER	LF1
390254-01	TRANSISTOR JFET MPF102/PN4302	Q321, Q331	252133-01	FERRITE BEAD LONG	FB802
902658-01	TRANSISTOR NPN 3904	Q501, Q711	903025-06	FERRITE BEAD LONG (SUB FOR 252133-01)	FB802
902707-01	TRANSISTOR PNP 3906	Q301, Q502, Q503	903025-08	FERRITE BEAD LONG (SUB FOR 252133-01)	FB802
900850-01	DIODE 1N4148	D501, D911, D912	252173-01	FERRITE BEAD RADIAL	E431-E433, E435
390017-01	DIODE 1N914 (SUB FOR 900850-01)	D501, D911, D912	903025-01	FERRITE BEAD AXIAL (SUB FOR 252173-01)	E431-E433, E435
252344-01	OSCILLATOR 28.37516 MHZ (PAL)	X1	366648-01	LABEL BAR CODE BLANK	
325566-14	OSCILLATOR 28.63636 MHZ (NTSC)	X1	366649-01	LABEL BAR CODE BLANK	
900560-01	CRYSTAL 32.768 HZ	Y9			
CAPACITORS					
251029-06	TRIMMER 6.8 PF - 45 PF	TC9			
390082-01	MLC AXIAL Z5U .01UF	C7-C8, C10, C12, C15, C32-C37, C39, C308, C701, C713, C800-C803			
390082-02	MLC AXIAL Z5U .1UF	C711			
390082-04	MLC AXIAL Z5U .33UF	C1-C6, C9, C11, C13, C14, C16-C20, C40-C42, C301, C302, C305, C325, C335, C501, C502, C804			
900462-21	MLC AXIAL NPO 22 PF	C911, E666			
900462-29	MLC AXIAL NPO 47 PF	E403, E102, E103, E106-E109, E791-E794			

**Commodore International Spare Parts List
A501 PLUS SHIPPING ASSEMBLIES**

Commodore part numbers are provided for reference only and do not indicate the availability of spare parts from Commodore. Industry standard parts (Resistors, Capacitors, Connectors) should be secured locally. Part number information may vary according to country, some parts may not be available in all countries. Part Numbers are subject to change, see Parts (Section 2) of current Techtopics for current numbers.

SHIP ASSY A501 PLUS		SHIP ASSY A501 PLUS (Continued)	
535009-01	SHIP ASSY A501 PLUS INTERNATIONAL	312602-01	TRAY BOX
364039-01	MAIN ASSY A501 PLUS	319120-03	BOX INDIVIDUAL
241006-04	BAG ANTI STATIC	368084-01	SEAL TAMPER EVIDENT
318778-02	BAG ANTI STATIC (SUB FOR 241006-04)	319200-03	BOX MASTER SHIPPING 1/4
368412-01	LEAFLET INSTRUCTION		

**Commodore International Spare Parts List
A501 PLUS MAJOR ASSEMBLIES**

Commodore part numbers are provided for reference only and do not indicate the availability of spare parts from Commodore. Industry standard parts (Resistors, Capacitors, Connectors) should be secured locally. Part number information may vary according to country, some parts may not be available in all countries. See Section 3 for Dis-assembly diagrams.

MAIN ASSY A501 PLUS		MAIN ASSY A501 PLUS (Continued)	
364039-01	MAIN ASSY A501 PLUS	312609-01	TAPE PRESSURE SENSITIVE
312606-01	TOP SHIELD	363834-01	PCB ASSEMBLY A501 PLUS
312608-01	BOTTOM SHIELD	366648-01	LABEL BAR CODE BLANK 0.5" X 1.75"
312607-01	INSULATION SHEET	366649-01	LABEL BAR CODE BLANK 0.5" X 1.00"

**Commodore International Spare Parts List
A501 PLUS PCB Components
PCB Assembly #363834**

Commodore part numbers are provided for reference only and do not indicate the availability of spare parts from Commodore. Industry standard parts (Resistors, Capacitors, Connectors) should be secured locally. Part number information may vary according to country, some parts may not be available in all countries.

IC COMPONENTS			RESISTOR NETWORKS		
318099-04	DRAM 256K X 4 120NS	U1-U8	390227-05	68 OHM SIP 10 PIN 5 ELEMENT	RP901-RP903
318099-02	DRAM 256K X 4 100NS (SUB FOR 318099-04)	U1-U8	MISCELLANEOUS		
CONNECTORS			366648-01	LABEL BAR CODE BLANK 0.5" X 1.75"	
380311-05	FEMALE HEADER 56 PIN R ANGLE	J9	366649-01	LABEL BAR CODE BLANK 0.5" X 1.00"	
CAPACITORS					
390082-04	MLC AXIAL 25U 0.33UF	C1-C8			
390101-02	ELEC ALUM RAD 100UF 16V	C902,C903			

JUMPERS AND STUFF

REF	TYPE	DESCRIPTION	PAGE
JP1	BLOB	KEYBOARD RESET	7
JP2	BLOB	CO VS. 08 ADDRESS MAP	2
JP3	BLOB	EXPANSION RAS SELECT	3
JP4	BLOB	BYPASS 2M-BYTE DECODER	3
JP7	BLOB	EXPANSION/TICK OPTION	6.8
JP8	BLOB	LIGHT PEN PORT SELECT	5
JP9	BLOB	ON-BOARD RTC BYPASS	8
JP10	BLOB	RS232 AUDIO I/O CUTOFF	5
JP11	BLOB	TTL VS RS170 COMP SYNC	4

CONNECTORS

REF	TYPE	DESCRIPTION	PAGE
CN1	DB9P	MOUSE/JOYSTICK 1	5
CN2	DB9P	MOUSE/JOYSTICK 2	5
CN3	RCA-J	RIGHT AUDIO OUTPUT	5
CN4	RCA-J	LEFT AUDIO OUTPUT	5
CN5	DB25S	EXTERNAL FLOPPY	7
CN6	DB25P	RS232 SERIAL PORT	6
CN7	DB25S	PARALLEL PRINTER PORT	6
CN8	SO DIN	POWER SUPPLY CONNECTOR	10
CN9	DB23P	VIDEO OUTPUT	4
CN10	RCA-J	COMPOSITE VIDEO	4
CN11	DIL-34	INTERNAL FLOPPY SIGNAL	7
CN12	SIL-4	INTERNAL FLOPPY POWER	7
CN13	SIL-8	KEYBOARD CONNECTOR	7
P1	EDGE86	EXPANSION CONNECTOR	9
P9	RA-56H	MEM. EXP. MAIN-BOARD	8

REVISION HISTORY

REV	DESCRIPTION	DATE	APRVL	MANAGER
-	FOR OLDER REVISION 3/5 BOARDS			
	SEE SCHEMATIC 312511-01			
-	FOR OLDER REVISION 6A/7 BOARDS			
	SEE SCHEMATIC 312007-01			
0	PCB RA ENGINEERING PROTOTYPE	04/13/91	GRR	
1	PCB RBA ADVANCED ENGINEERING RELEASE	06/20/91	GRR	<i>GRR</i>

SIGNAL GLOSSARY

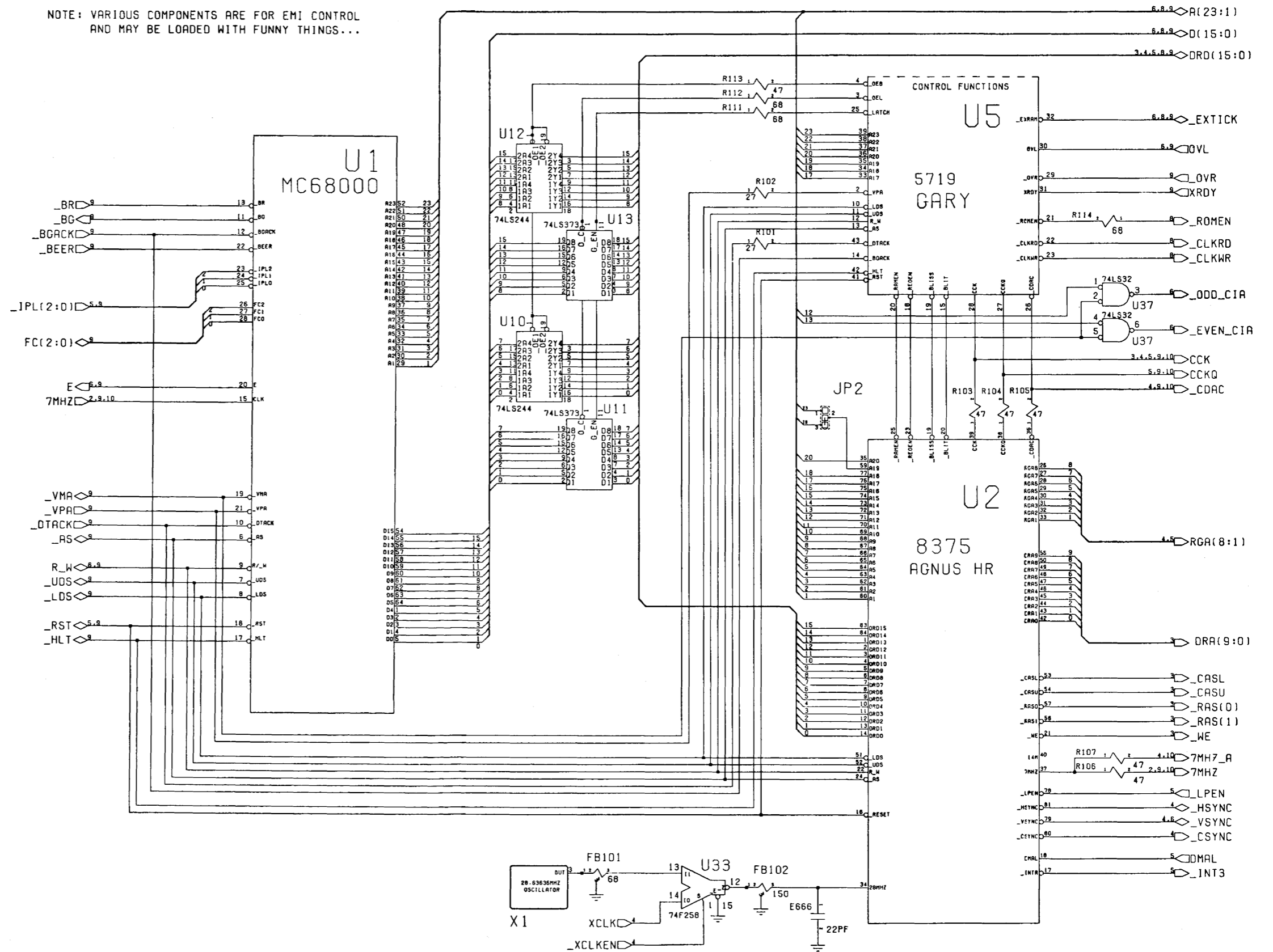
SIGNAL	DESCRIPTION (AREA)	PAGES
28MHZ	28.63636 MHZ MASTER CLOCK	2
7MHZ	7.15909 MHZ PROCESSOR CLOCK	2,4,9,10
A[23:1]	PROCESSOR ADDRESS BUS (68000)	2,6,8,9
ACK	DATA ACKNOWLEDGE (PARALLEL PORT)	6
AS	ADDRESS STROBE (68000)	2,9
AUDIN	AUDIO INPUT (RS232 PORT)	5,6
AUDOUT	AUDIO OUTPUT (RS232 JACK)	5,6
BEER	BUS ERROR (68000)	2,9
BG	BUS GRANT (68000)	2,9
BGACK	BUS GRANT ACKNOWLEDGE (68000)	2,9
BLISS	BLITTER SLOWDOWN (CHIPS)	2
BLIT	CHIP MEMORY ACCESS (CHIPS)	2
BR	BUS REQUEST (68000)	2,9
BUSY	DEVICE BUSY (PARALLEL PORT)	6
CASL/U	COLUMN ADDRESS STROBE (DRAM)	2,3
CCK/CCKQ	COLOR CLOCK / QUADRATURE (CHIPS)	2-5,9,10
CDAC	7.15909 MHZ QUADRATURE CLOCK (CHIPS)	2,4,9,10
CHNG	MEDIA CHANGE (FLOPPY)	6,7
CLKRD/WR	READ-TIME CLOCK READ / WRITE (RTC)	2,8
COMP	MONOCHROME COMPOSITE VIDEO (VIDEO)	4
CSYNC	COMPOSITE SYNC (VIDEO)	2,4
CIS	CLEAR IO SEND (RS232 PORT)	6
D[15:0]	PROCESSOR DATA BUS (68000)	2,6,8,9
DIR	STEP DIRECTION (FLOPPY)	6,7
DKRD	DISK READ DATA (FLOPPY)	5,7
DKWD	DISK WRITE DATA (FLOPPY)	5,7
DKWE	DISK WRITE ENABLE (FLOPPY)	5,7
DMAL	CHIP DMA REQUEST LINE (CHIPS)	2,5
DRA[8:0]	DRAM ADDRESS BUS (DRAM)	2,3
DRD[15:0]	DRAM DATA BUS (DRAM)	2-5,8,9
DSR	DATA SET READY (RS232 PORT)	6
DTACK	DATA TRANSFER ACKNOWLEDGE (68000)	2,9
DTR	DATA TERMINAL READY (RS232 PORT)	6
E	PERIPHERAL ENABLE CLOCK (68000)	2,6,9
EXTICK	EXPANSION PRESENT / RTC TICK	2,6,8,9
FC[2:0]	FUNCTION CODE (68000)	2,9
FIREQ/1	FIRE BUTTON Q/1 (JOYSTICKS)	5,6
HIT	PROCESSOR HALT (68000)	2,9
HSYNC	HORIZONTAL SYNC (VIDEO)	2,4,6
INDEX	INDEX PULSE (FLOPPY)	6,7
INT[2,3,6]	INTERRUPT REQUEST (CHIPS)	2,5,6,9
IORSET	I/O RESET	6,7,9
IPL[2:0]	INTERRUPT PRIORITY LEVEL (68000)	2,5,9
KBCLOCK	KEYBOARD CLOCK (KEYBOARD)	6,7
KBDATA	KEYBOARD DATA (KEYBOARD)	6,7
KBRESET	KEYBOARD RESET (KEYBOARD)	7
LDS/UDS	UPPER / LOWER DATA STROBES (68000)	2,9
LED	POWER ON LED / AUDIO FILTER DISABLE	5,6,7
LEFT/RIGHT	LEFT RIGHT AUDIO (AUDIO)	5

SIGNAL	DESCRIPTION (AREA)	PAGES
LPEN	LIGHT PEN TRIGGER (JOYSTICKS)	2,5
MTR	MOTOR ON (FLOPPY)	6,7
MTR0	MOTOR ON - DRIVE 0 (FLOPPY)	7
MOV/MOH	MOUSE 0 QUADRATURE V/H (JOYSTICKS)	4,5
MIV/MIH	MOUSE 1 QUADRATURE V/H (JOYSTICKS)	4,5
OVL	OVERLAY ROM OVER RAM	2,6,9
OVR	OVERRIDE SYSTEM DECODING	2,9
PIXELSW	GENLOCK PIXEL SWITCH (VIDEO)	4
POTX/OY	POT LINES 0 X/Y (JOYSTICKS)	5
POTIX/IY	POT LINES 1 X/Y (JOYSTICKS)	5
POUT	PAPER OUT (PARALLEL PORT)	6
PPD[7:0]	PARALLEL PORT DATA (PARALLEL PORT)	6
RAMEN	RAM ENABLE (CHIPS)	2
REGEN	CHIP REGISTER ENABLE (CHIPS)	2
RAS0/1	ROW ADDRESS STROBE (DRAM)	2,3
RDY	DRIVE READY (FLOPPY)	6,7
RESET	GENERAL RESET	6,9
RGA[8:1]	REGISTER ADDRESS BUS (CHIPS)	2,4,5
R/G/B	RED / GREEN / BLUE (VIDEO)	4
RI	RING INDICATE (RS232 PORT)	6
ROMEN	ROM ENABLE (ROM)	2,8
RTS	REQUEST TO SEND (RS232 PORT)	6
RST	PROCESSOR RESET (68000)	2,5,9
RXD	RECEIVE DATA (RS232 PORT)	5,6
RW	PROCESSOR READ/WRITE (68000)	2,6,9
SEL	SELECT (PARALLEL PORT)	6
SEL[3:0]	DRIVE SELECT (FLOPPY)	6,7
SIDE	SIDE SELECT (FLOPPY)	6,7
STEP	STEP IN/OUT COMMAND (FLOPPY)	6,7
TRKO	TRACK ZERO SENSE (FLOPPY)	6,7
TXD	TRANSMIT DATA (RS232 PORT)	5,6
VMA	VALID MEMORY ADDRESS (68000)	2,9
VPA	VALID PERIPHERAL ADDRESS (68000)	2,9
VSYNC	VERTICAL SYNC (VIDEO)	2,4,6
WE	WRITE ENABLE (DRAM)	2,3
WPROT	WRITE PROTECT SENSE (FLOPPY)	6,7
XCLK	EXTERNAL GENLOCK CLOCK (VIDEO)	2,4
XCLKEN	EXTERNAL CLOCK ENABLE (VIDEO)	2,4,9
XRDY	EXTERNAL DATA READY	2,9

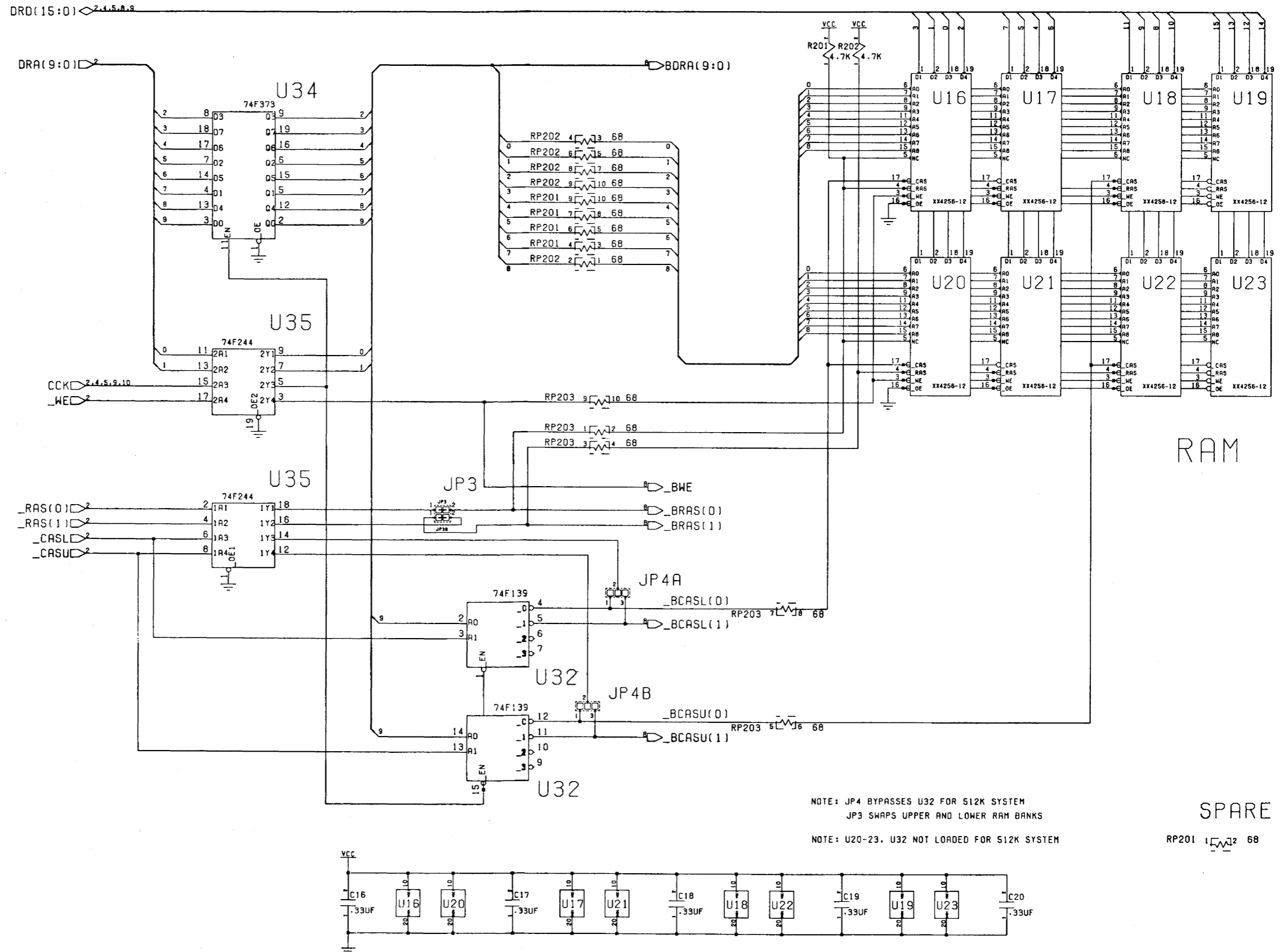
KEY COMPONENTS

REF	CHIP	DESCRIPTION	PAGE
U1	68000	68000 PROCESSOR, 8MHZ	2
U2	8375	AGNUS HR	2
U3	8364	PAULA	5
U4	8373	DENISE HR	4
	8362	DENISE	0BS
U5	5719	GARY	2,7
U6	ASST	ROM 256KX16, 200 NS	8
U7-8	8520	AMIGA VIA, 1 MHZ	6
U9	6242	REAL TIME CLOCK	8
U14	LF347	BIMOS OP-AMP	5
	TL084	BIMOS OP-AMP	ALT
U38	1488	EIA LINE DRIVER	6
U39	1489	EIA LINE RECEIVER	6
U42	NE555	TIMER	7
U16-19	ASST	DRAM 256KX4, 120 NS	3
U20-23	ASST	DRAM 256KX4, 120 NS	3
X1	OSC	TTL 28.63636 MHZ NTSC	2
	OSC	TTL 28.37512 MHZ PAL	ALT
HY1	ASST	VIDEO HYBRID	4

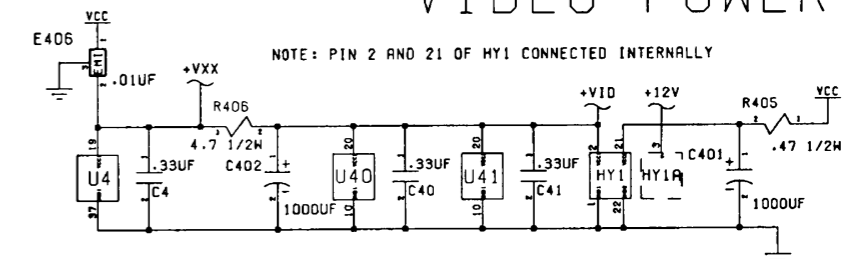
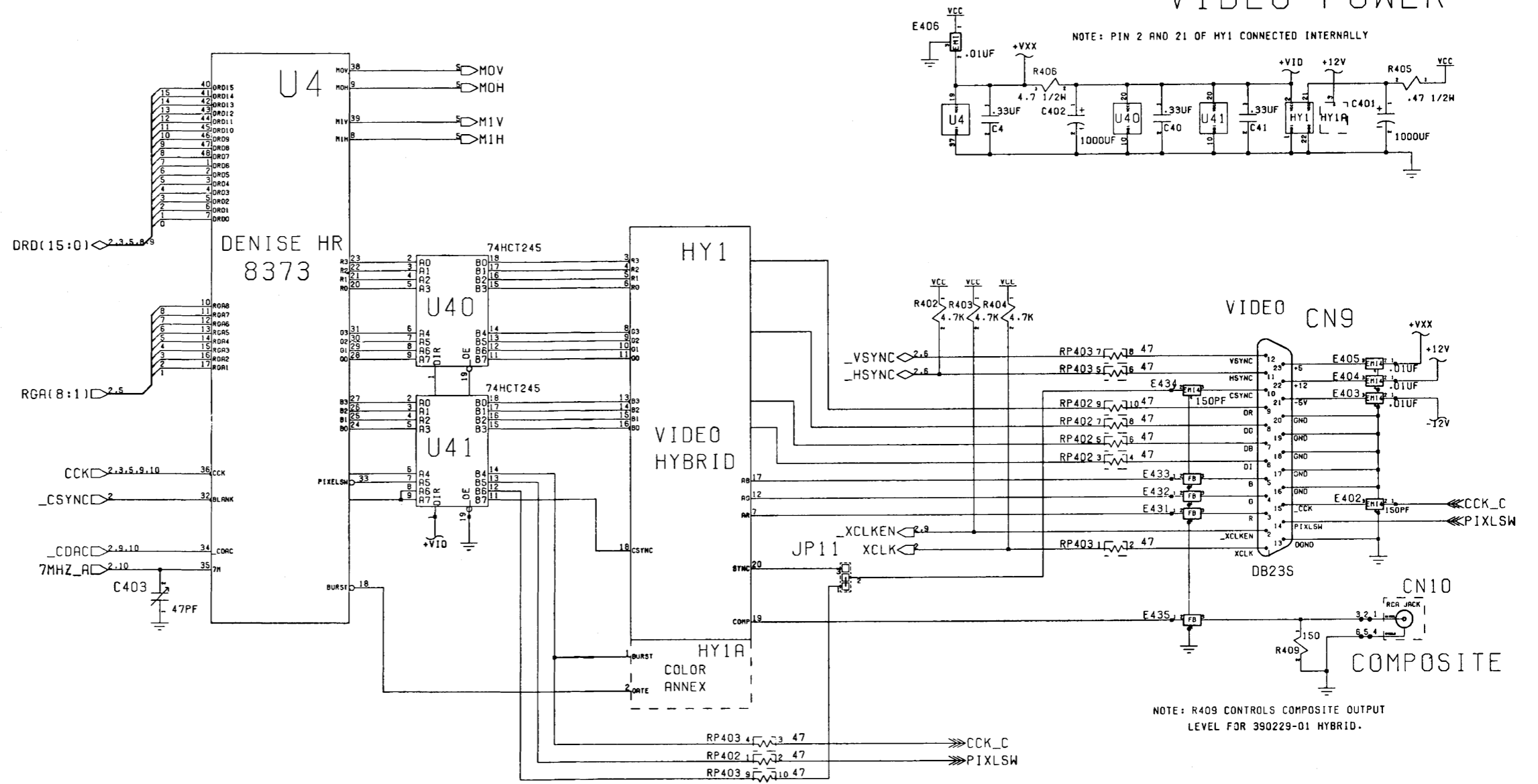
NOTE: VARIOUS COMPONENTS ARE FOR EMI CONTROL
AND MAY BE LOADED WITH FUNNY THINGS...



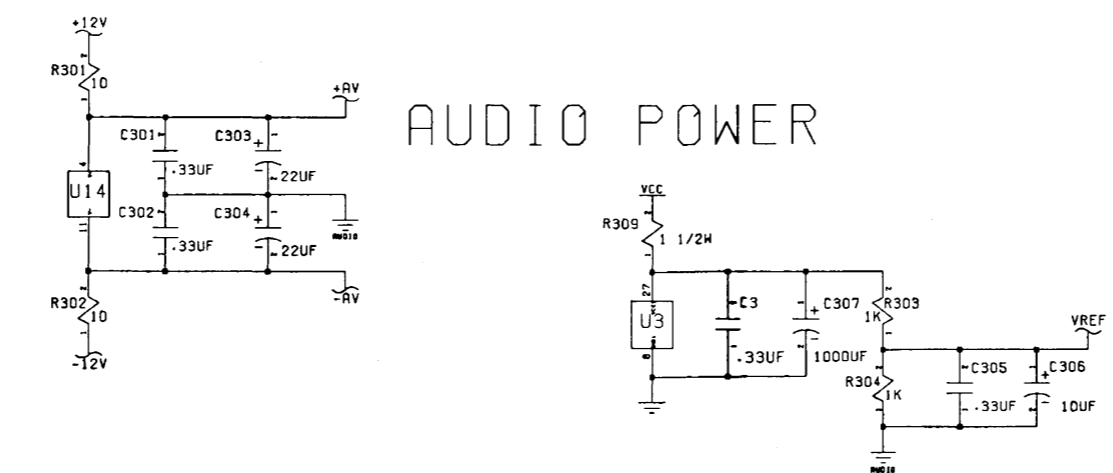
NOTE: PAL USES 28.37516 MHZ



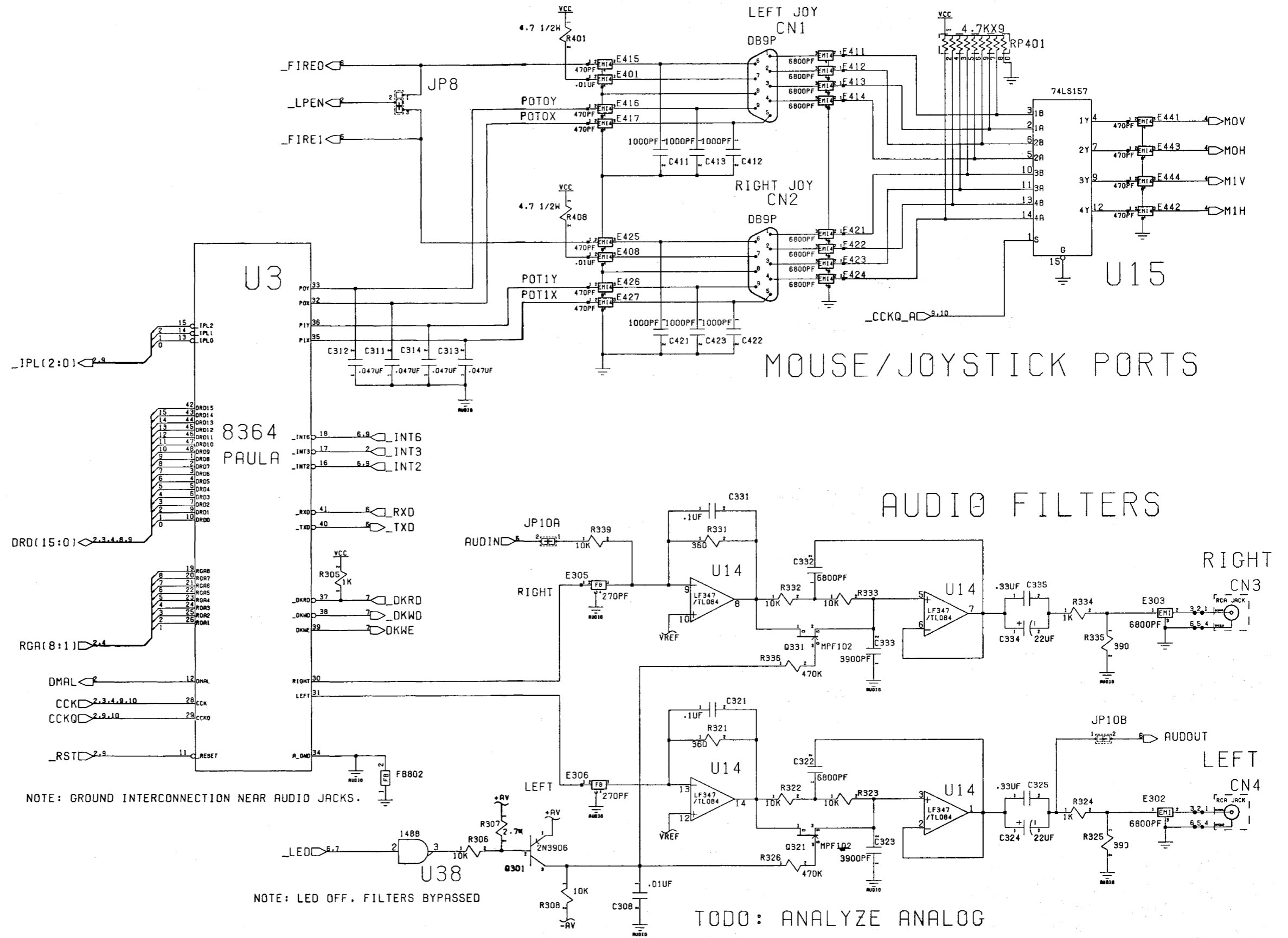
VIDEO POWER



AUDIO POWER



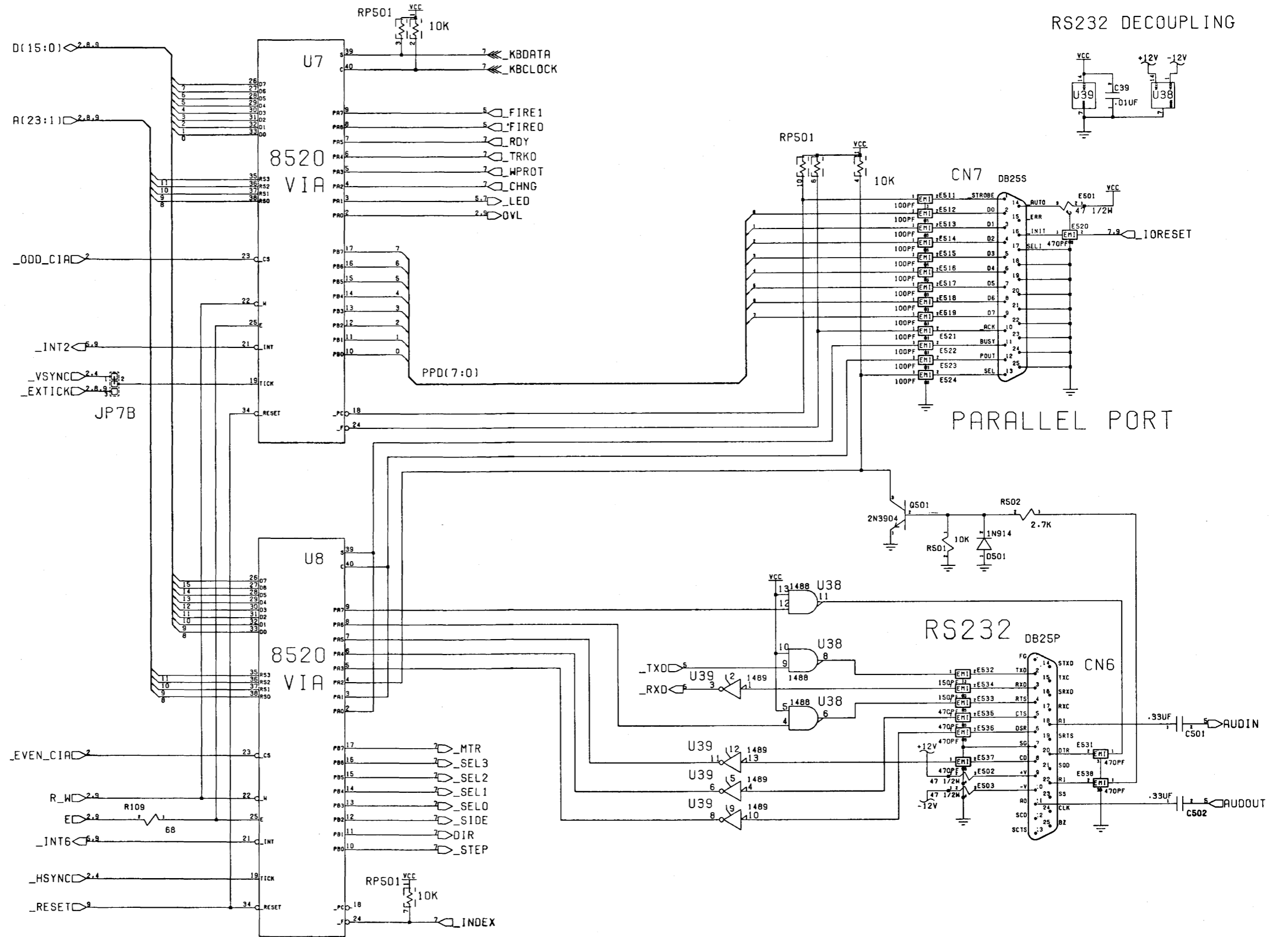
NOTE: COMPONENTS DESIGNATED AS EXXX MAY BE LOADED WITH EMI FILTERS, FERRITE BEADS OR RESISTORS!



NOTE: GROUND INTERCONNECTION NEAR AUDIO JACKS.

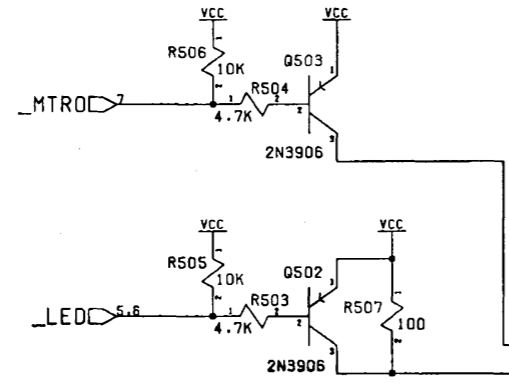
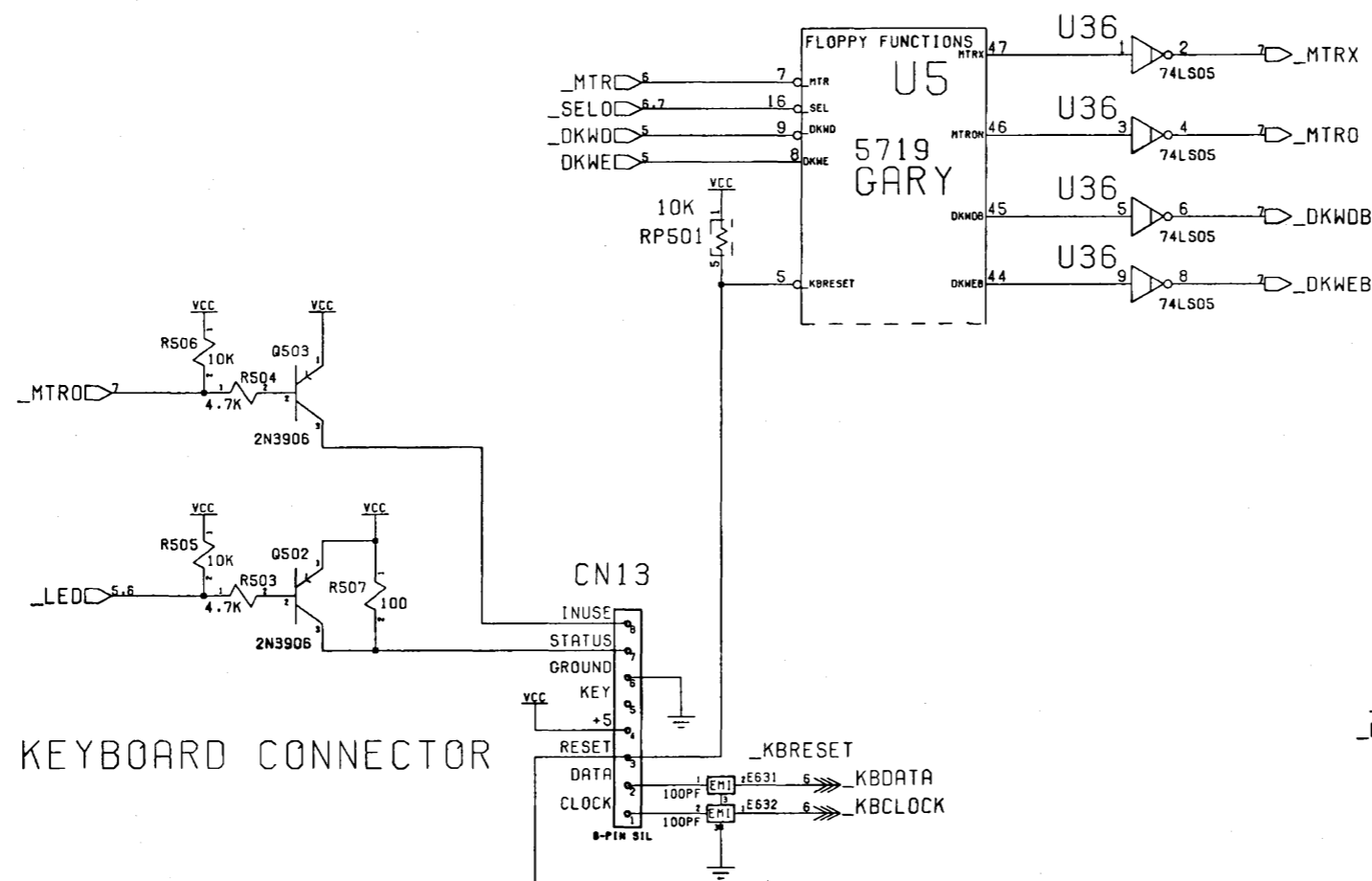
NOTE: LED OFF, FILTERS BYPASSED

TODO: ANALYZE ANALOG

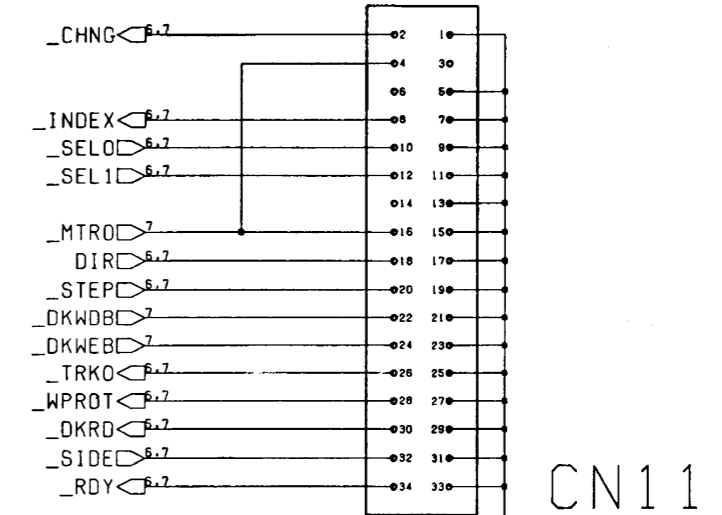


NOTE: E501-S03 ARE LOADED WITH 47 OHM 1/2 W RESISTORS

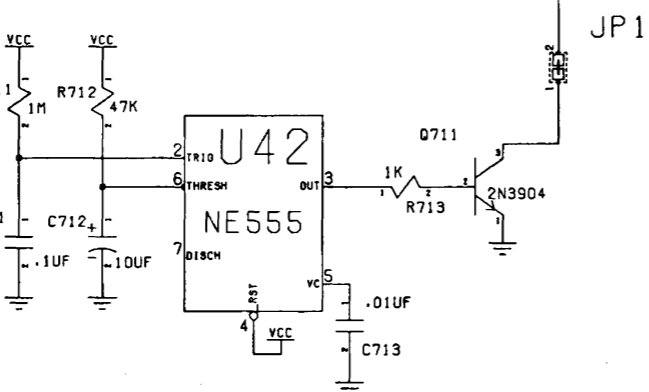
FLOPPY LOGIC



KEYBOARD CONNECTOR

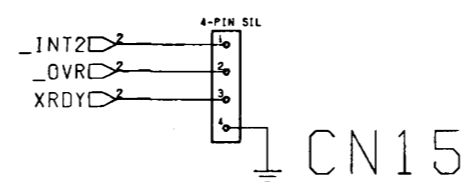


INTERNAL FLOPPY

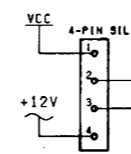


POWER UP RESET

IDE I/F

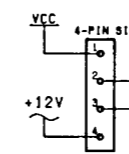


IDE POWER

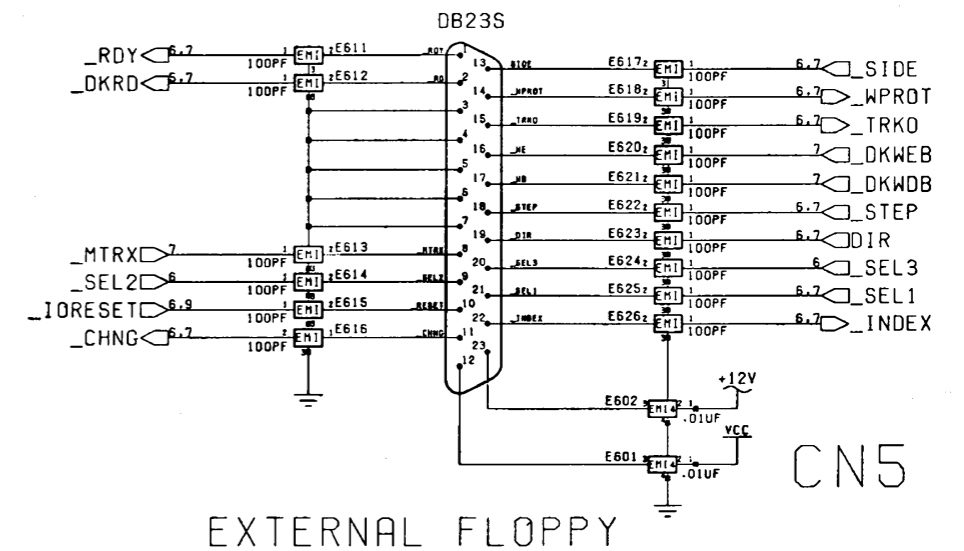


CN14

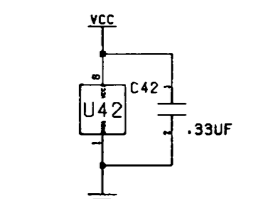
FLOPPY POWER



CN12



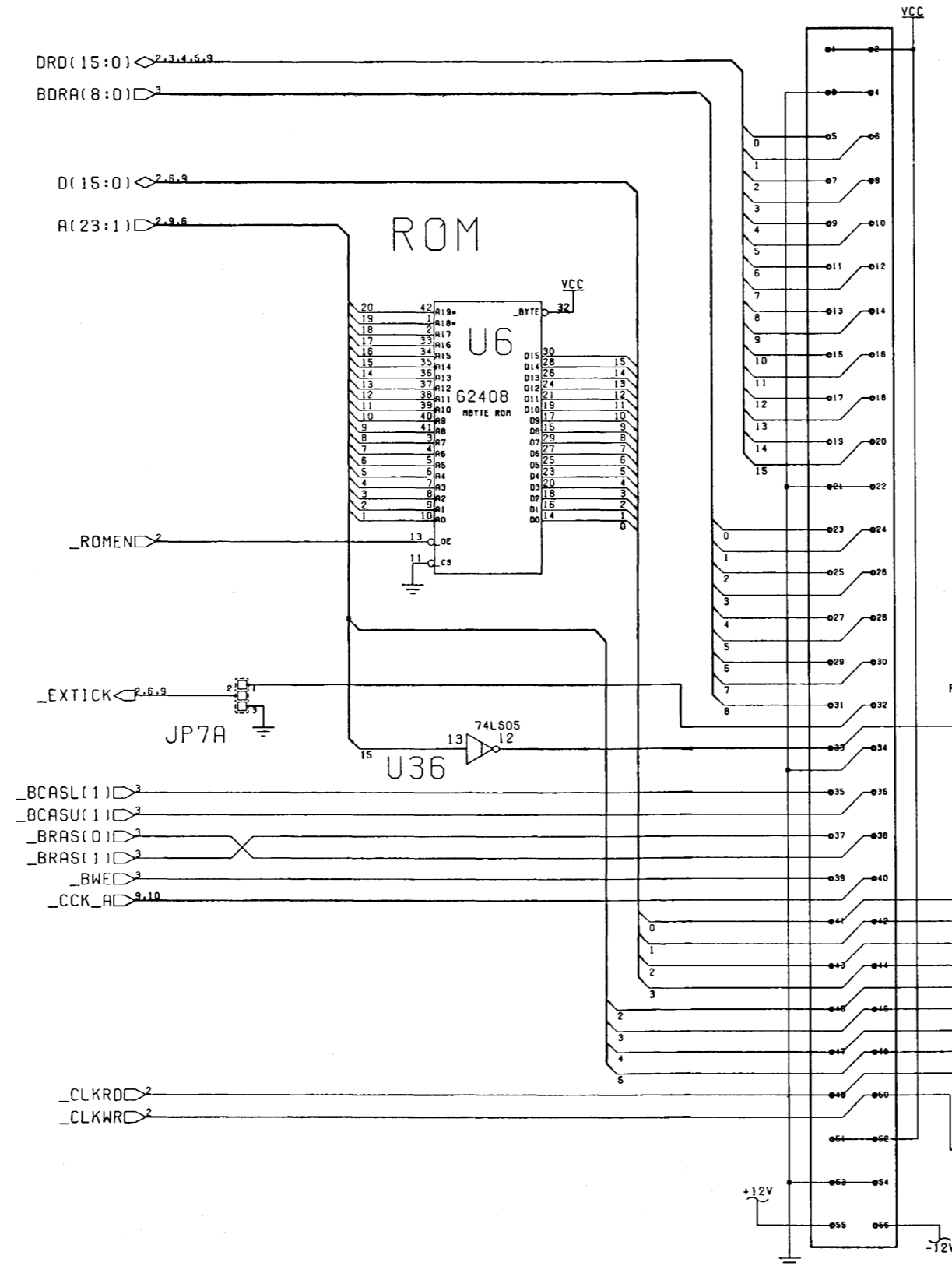
EXTERNAL FLOPPY



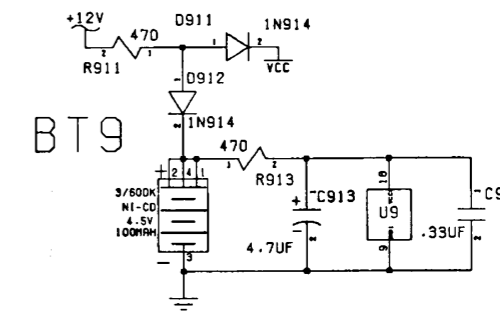
DECOUPLING

NOTE: SOME DRIVES ARE +5 ONLY...

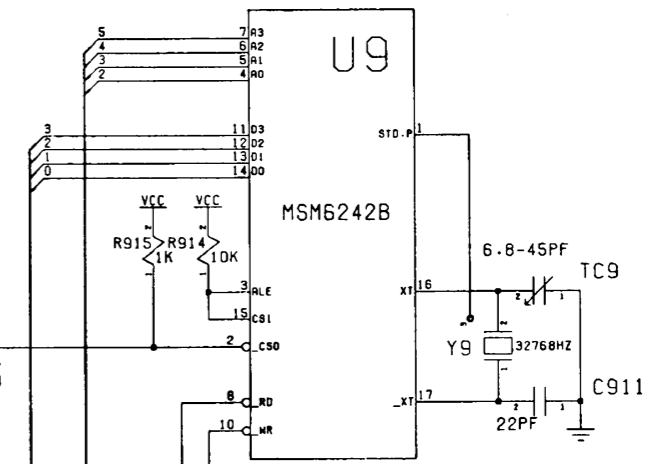
MEMORY EXPANSION



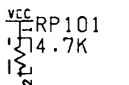
REAL TIME POWER



REAL TIME CLOCK

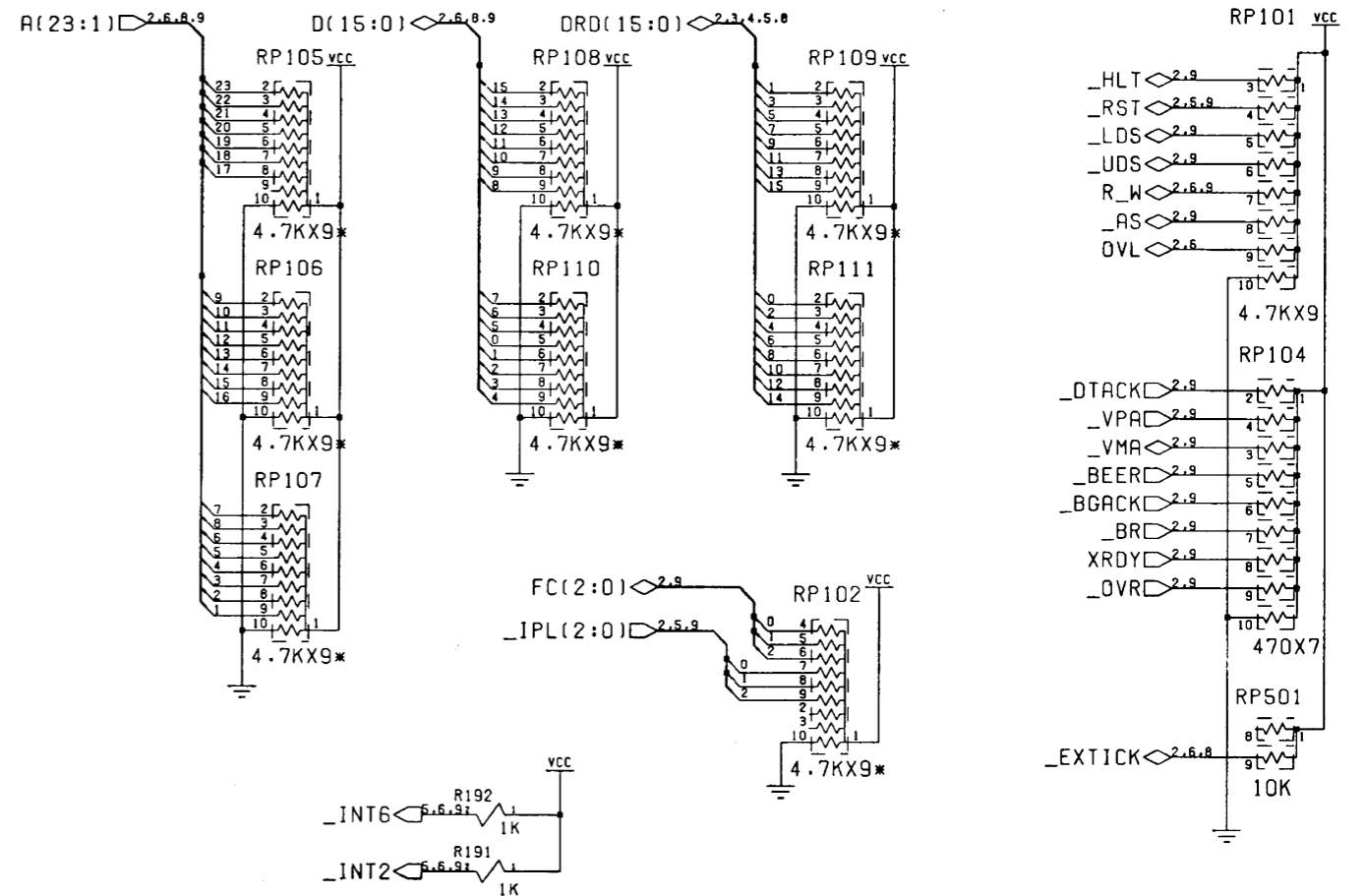
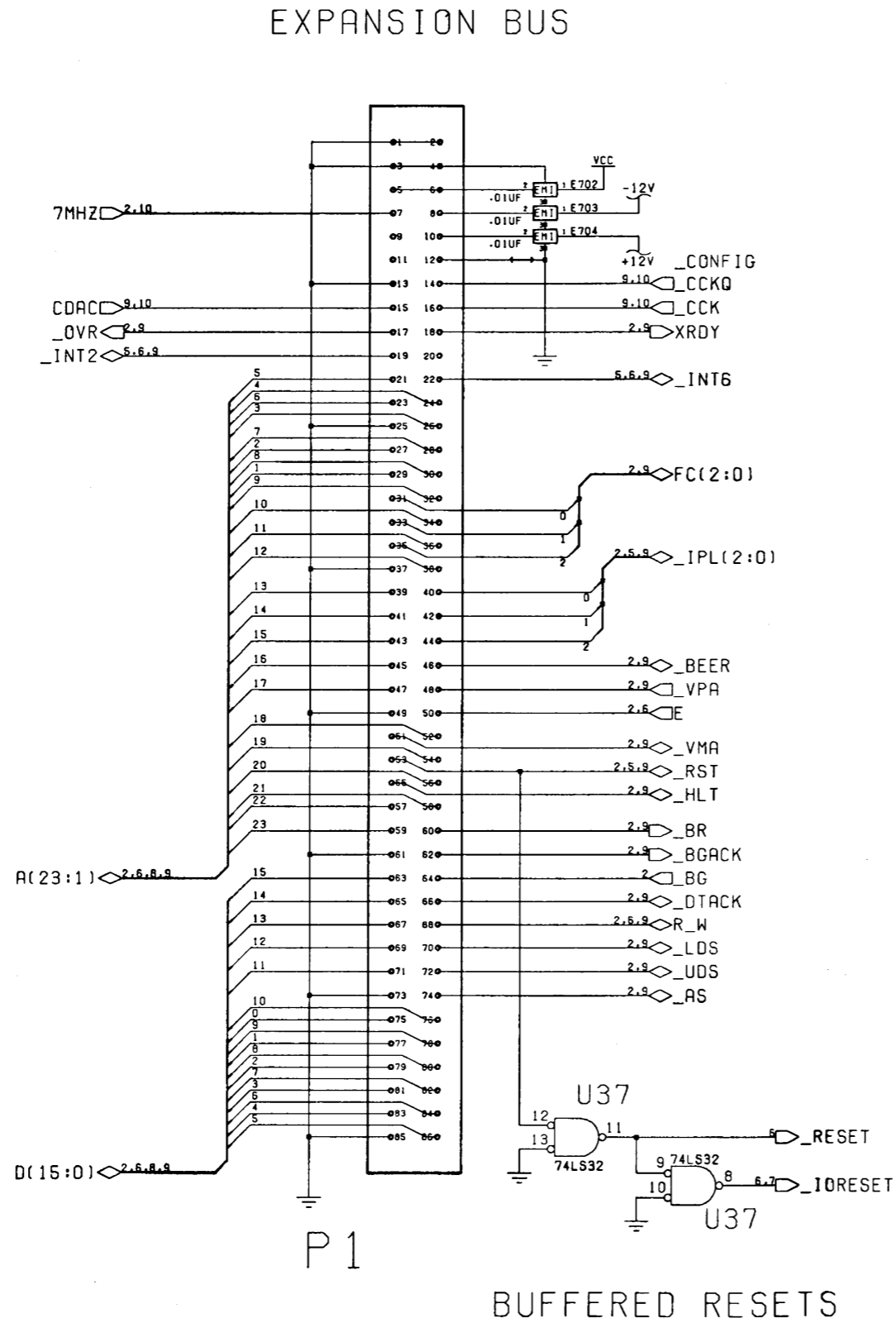


SPARE

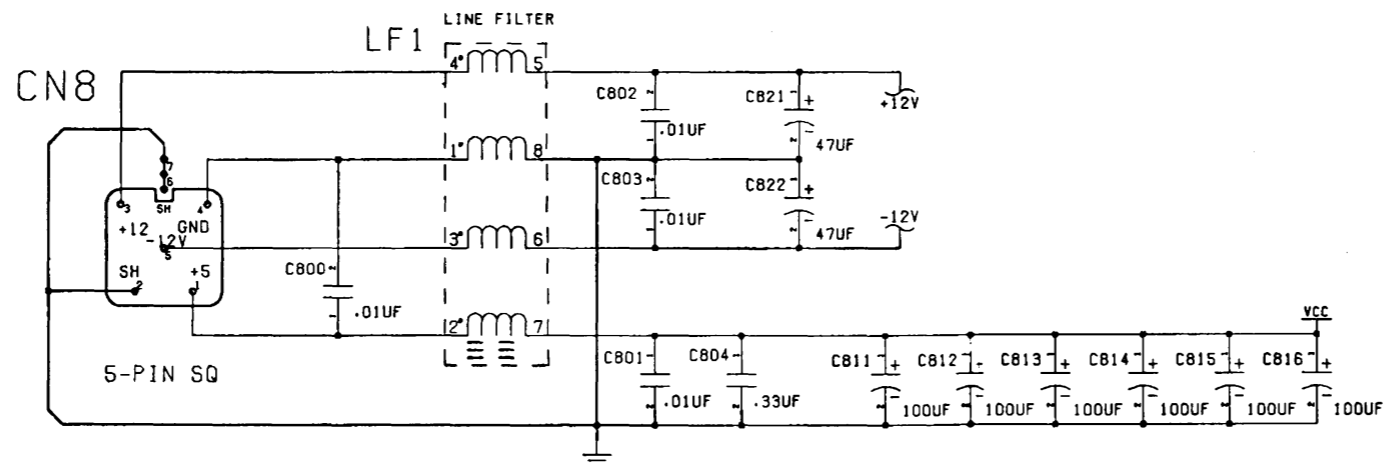


NOTE: ONLY 4/8 M-BIT ROM USES PIN 1 AND 42

EXPANSION BUS TERMINATION AND PULLUPS

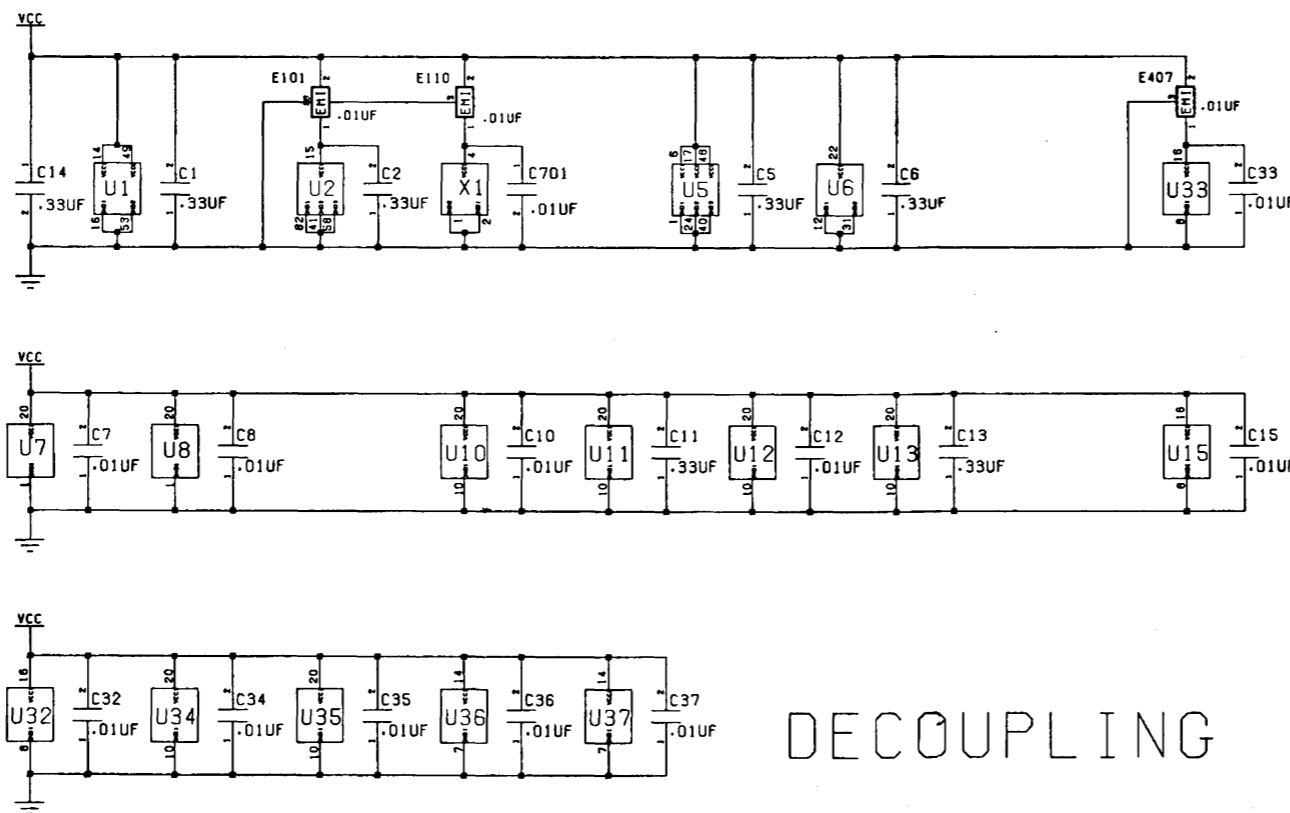
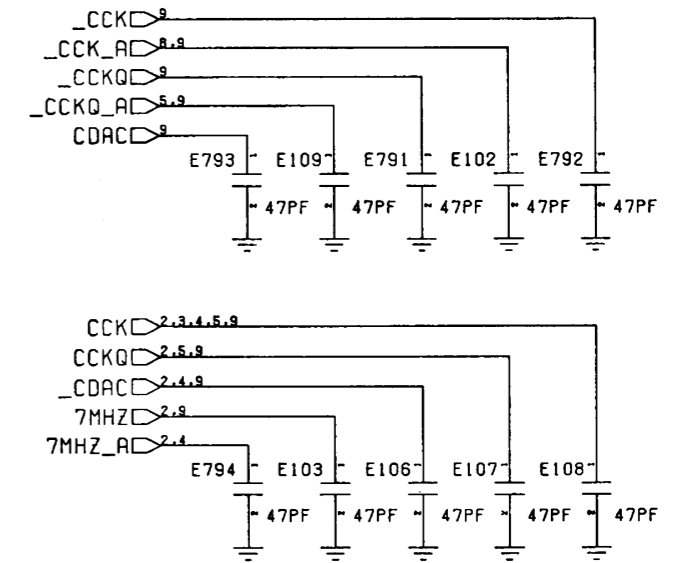


POWER INPUT



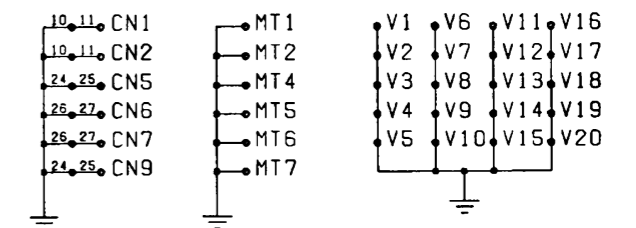
NOTE: HEAVY LINES INDICATE A SINGLE POINT CONNECTION

FCC GOOBERS

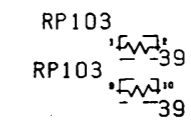


DECOUPLING

GROUNDING HOLES, & C.



SPARES



JUMPERS AND STUFF

REF	TYPE	DESCRIPTION	PAGE
JP1	BLOB	MEMORY EXPANSION SENSE	3
JP2	BLOB	REFRESH KLUDGE BYPASS	2
JP3	BLOB	EXPANSION RAS SELECT	2
JP9	BLOB	RTC SELECT DISABLE	3

CONNECTORS

REF	TYPE	DESCRIPTION	PAGE
J9		56-RAFHMEN. EXP. MAIN-BOARD	3

REVISION HISTORY

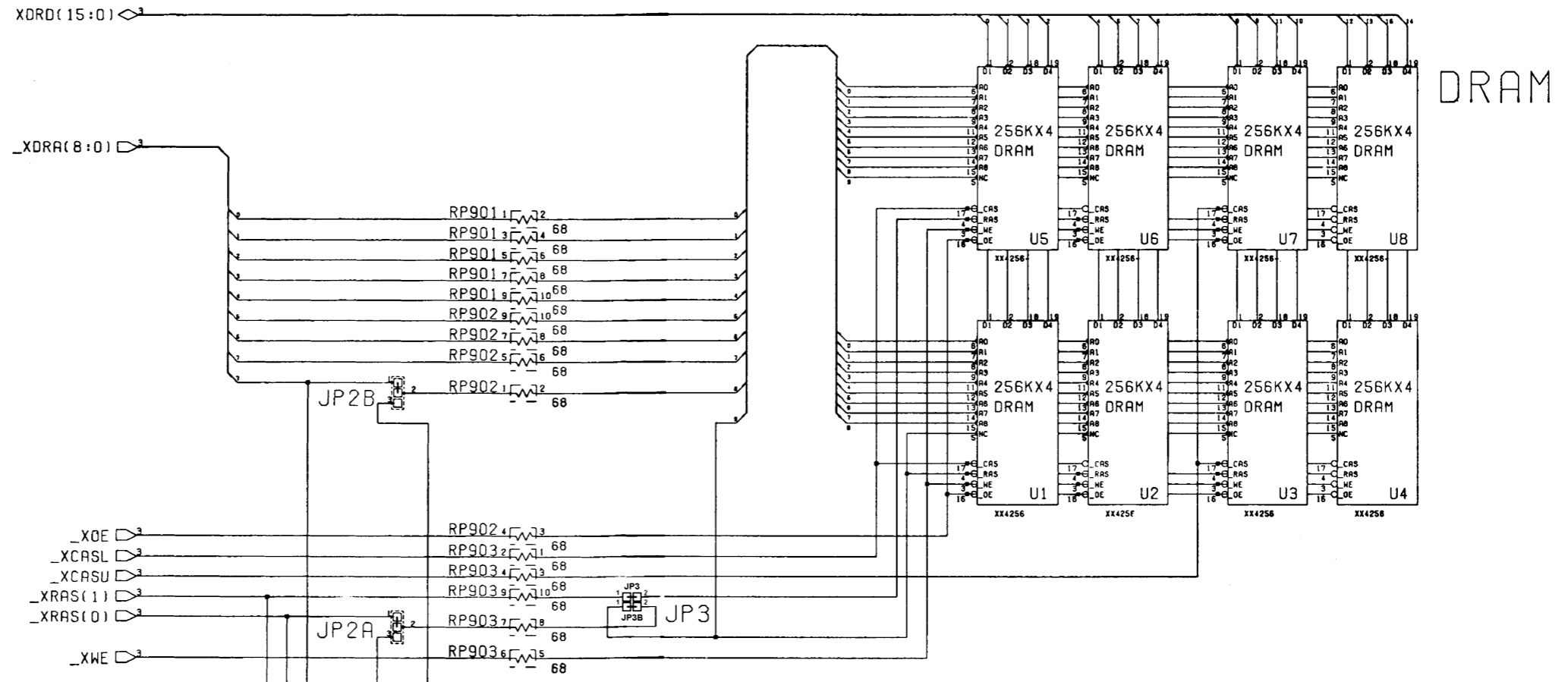
REV	DESCRIPTION	DATE	APRVL	MANAGER
-	FOR OLDER REVISION 3/5 BOARDS SEE SCHEMATIC 312511-01			
-	FOR OLDER REVISION 6C BOARDS SEE SCHEMATIC 312988-01			
0	PCB A501+ R8 ENGINEERING PROTOTYPE	06/18/91	GRR	
1	ADVANCE ENGINEERING RELEASE	7/19/91	GRR	G.R.

SIGNAL GLOSSARY

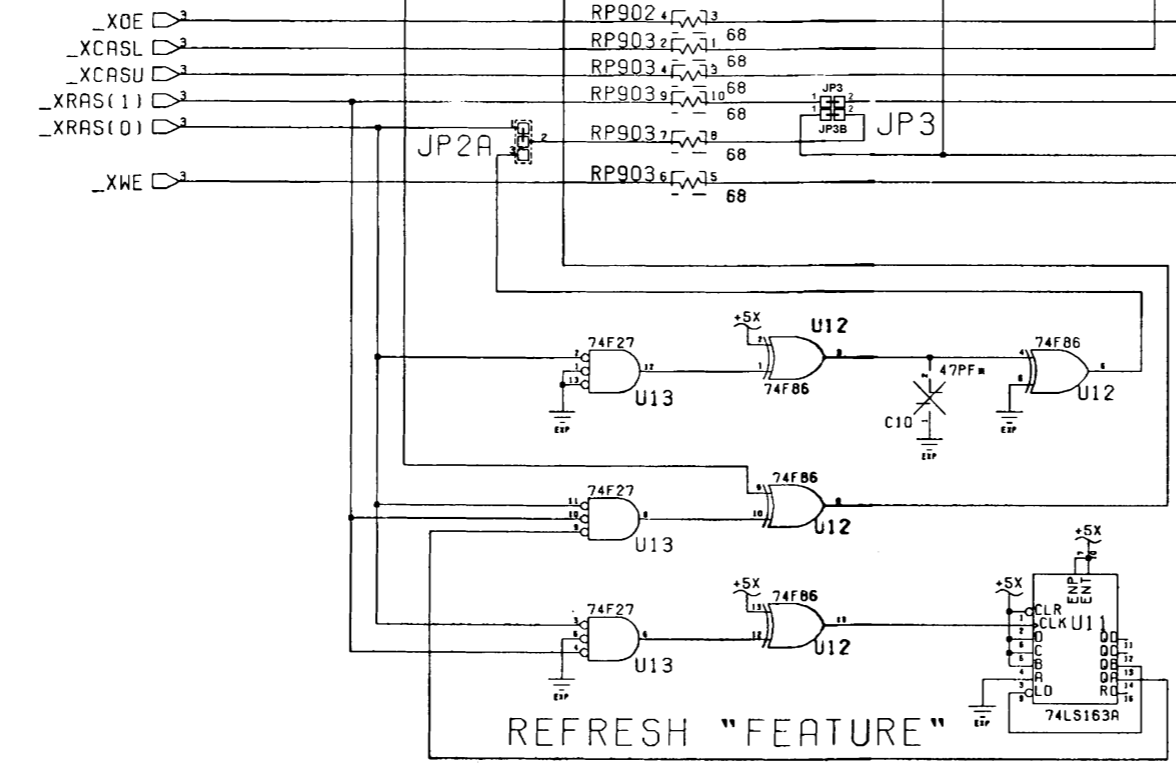
SIGNAL	DESCRIPTION (AREA)	PAGES
A[23:1]	PROCESSOR ADDRESS BUS (68000)	3
D[15:0]	PROCESSOR DATA BUS (68000)	3
CASL/U	COLUMN ADDRESS STROBE (DRAM)	2,3
CCK/CCKQ	COLOR CLOCK / QUADRATURE (CHIPS)	3
CLKRD/WR	REAL TIME CLOCK READ / WRITE (RTC)	3
CLKCS	REAL TIME CLOCK CHIP SELECT (RTC)	3
DRAL[8:0]	DRAM ADDRESS BUS (DRAM)	2,3
DRD[15:0]	DRAM DATA BUS (DRAM)	2,3
RASQ/1	ROW ADDRESS STROBE (DRAM)	2,3

KEY COMPONENTS

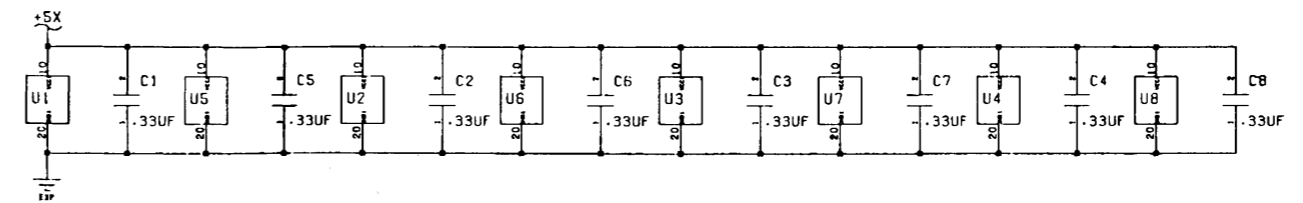
REF	CHIP	DESCRIPTION	PAGE
U1-U4	ASST	DRAM 256KX4, 120 NS	3
U5-U8	ASST	DRAM 256KX4, 120 NS	3
U9	6242	REAL TIME CLOCK	8
			5

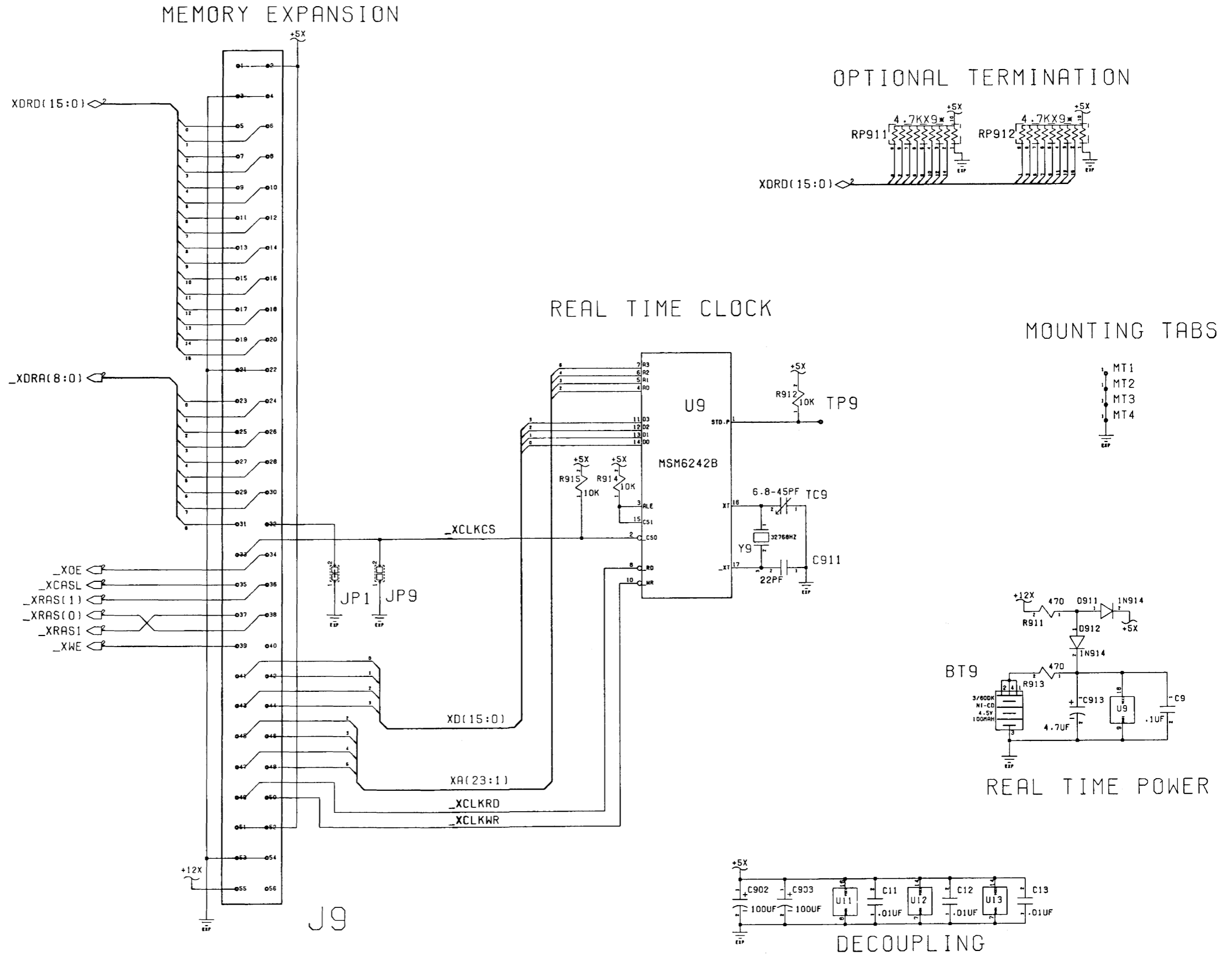


DRAM



NOTE: U5-U8 ARE ONLY LOADED FOR A501+ CONFIGURATION
U11-U13 ARE ONLY LOADED FOR A501 COMPATIBILITY
U1-U4 ARE GENERIC 256K-BIT X 4 120 NS DRAM
C10 IS OPTIONAL A8/RAS SETUP TIME CONTROL
RP911,RP912 ARE OPTIONAL DRD TERMINATION
TP9 IS CLOCK CALENDAR FREQUENCY TEST POINT





NOTE: REAL TIME CLOCK COMPONENTS ARE ONLY LOADED FOR A501 COMPATIBILITY